Développement et caractérisation d'un ASIC de lecture de macro-cellule de photo-détecteurs de grande dimension

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Thèse

Développement et caractérisation d'un ASIC de lecture de macro-cellule de photo-détecteurs de grande dimension

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Résumé

PMm² est un projet financé pour 3 ans (2007-2010) par l'Agence Nationale de la Recherche (ANR) dont le titre exact est "Electronique innovante pour photo-détecteurs distribués en physique des particules et astroparticule". Le projet regroupe les partenaires suivants: le LAL, l'IPN Orsay, le LAPP et une collaboration avec l'Université libre de Bruxelles (ULB).
La couverture de très grandes surfaces de photo-détection est un élément essentiel des dispositifs expérimentaux dévolus aux études des gerbes atmosphériques de grande énergie, des neutrinos de différentes sources (soleil, atmosphérique, supernova, réacteurs, accélérateurs).
La prochaine génération d'expériences, comme l'après Super-Kamiokande ou tous les détecteurs Cerenkov à eau de très grande taille, ne pourront plus baser leur construction seulement sur un simple agrandissement des expériences existantes, pour améliorer les performances de détection. Ils doivent concentrer leurs efforts de R&D sur la réduction de la complexité.
L'objectif de ce projet est donc une "recherche amont" en vue de facilité la réalisation de grands détecteurs utilisant des milliers de photomultiplicateurs (PMTs).

Le projet PMm² propose de segmenter les grandes surfaces de photo-détection en "macro modules" de 16 PMTs de 12-inch (2x2 m²), connectés à une électronique innovante autonome qui fonctionne en déclenchement automatique et est installée proche des PMTs.
Ce développement est rendu possible par les progrès de la microélectronique qui permettent d'intégrer la lecture et le traitement des signaux de tous ces photomultiplicateurs à l'intérieur d'un même circuit intégré (ASIC) baptisé PARISROC (Photomultiplier ARray Integrated in SiGe Read Out Chip) et seules les données numérisées sont ensuite transmises par réseau vers le système de stockage des données en surface.

Le circuit PARISROC, réalisé en technologie AMS SiGe 0.35 µm, contient 16 voies totalement indépendantes correspondant aux 16 PMTs de chaque module. Chacune de ces voies permet la lecture de la charge du signal reçu ainsi que du temps associé.
La voie pour la mesure de charge est réalisée par un préamplificateur de tension et un "shaper" lent (200 ns) qui permet de mettre en forme le signal. Le signal obtenu est ensuite stocké dans une mémoire analogique, avant d'être converti en signaux numériques grâce à un convertisseur analogique numérique (ADC).
La voie pour la mesure de temps est, quant à elle, réalisée à partir du même préamplificateur suivi d'un "shaper" rapide (15ns) et d'un discriminateur. Grâce à un système de TDC (Time to Digital Converter) qui permet de convertir l'amplitude en temps, la mesure de temps est stockée dans une mémoire analogique, en parallèle de la charge, avant d'être convertie en signaux numériques.
Une des innovations de PARISROC, est la partie numérique compilée, incluse dans l'ASIC pour gérer les compteurs, l'échantillonnage des signaux, leur conversion ainsi que la transmission des données.
Le premier prototype du circuit PARISROC a une surface totale de 19 mm². Il a été envoyé en fabrication en juin 2008 chez Austrian Micro-System (AMS) par l'intermédiaire du centre de multi-projet CMP (à Grenoble), puis livré au laboratoire en décembre 2008.

Les mesures effectuées sur l'ASIC ont conduit à la réalisation d'un second prototype. Des améliorations notables ont été apportées, en termes de bruit, de dynamique, de vitesse de lecture du circuit (augmentation des horloges de 10 MHz à 40 MHz), de mesure de temps (améliorations de la TDC), de mesure de charge (améliorations du "shaper" lent).
Envoyé en fabrication en novembre 2009 et reçu au laboratoire en février 2010, ce nouveau prototype PARISROC 2 a été testé en laboratoire et l'analyse a montré un comportement répondant aux besoins du projet et la réalisation des modifications apportées.

Abstract

PMm² is a project funded for three years by the French National Agency for Research (ANR) with the complete title: "Innovative electronics for photo-detectors array used in high energy physics and astroparticles". The R&D is carried out by three laboratories: the LAL, the IPN Orsay, the LAPP and collaboration with the Université Libre de Bruxelles (ULB).
The coverage of large areas of photo-detection is a crucial element of experiments studying high energy atmospheric cosmic showers and neutrinos from different sources (sun, atmospheric, supernova, reactor and accelerator).
The next generation of experiments, such as the post-Super-Kamiokande detector or all the Water Cerenkov detector of large dimensions, could not base their programs only on a simple enlargement of existing experiments to improve the detection performance but they must concentrate their efforts on the new R&D programs of complexity reduction.
The objective of this project is thus an "upstream research" to realize big detectors using thousands of photomultipliers (PMTs).

The project proposes to segment the large surface of photo-detection into macro pixels consisting of an array of 16 PMTs of 12-inches (2*2 m²), connected to an autonomous front-end electronics which works in a triggerless data acquisition mode placed near the array.
This is possible thanks to the microelectronics progress that allows to integrate the readout and the signal processing, of all the photomultipliers, in the same circuit (ASIC) named PARISROC (Photomultiplier ARray Integrated in SiGe Read Out Chip). The ASIC must only send out the digital data by network to the surface central data storage.

The PARISROC Chip, made in AMS' Silicon Germanium (SiGe) 0.35 µm technology, integrates 16 independent channels for each PMTs of the array, providing charge and time measurements.
The charge channel is made by a voltage preamplifier and a slow shaper (up to 200 ns) to shape the input signal. The signal is then saved in the analog memory and converted to digital data thanks to an internal ADC (Analog to Digital Converter).
The time channel is made by a fast shaper (15 ns) followed by a discriminator. Thanks to a TDC (Time to Digital Converter), that converts the amplitude in time, the signal is saved in the analog memory, in parallel with the charge, and converted to digital data by the ADC.
One innovation is the digital part of PARISROC included in the ASIC to manage the counters, the signal sampling, their conversions and the data transmission.
The first prototype of PARISROC chip has a total surface of 19 mm². It has been sent for fabrication in June 2008 to AMS foundry (AustriaMicroSystems) through the CMP (Multi Project Center) and received in December 2008.

The ASIC measurements have led to the realization of a second prototype. Important measurements were brought in terms of noise, dynamic range, readout frequency (from 10 MHz to 40 MHz), time measurements (TDC improvements) and charge measurements (Slow shaper improvements).
Sent for fabrication in November 2009 and received in February 2010, this new prototype PARISROC 2 has been tested and the characterisation has shown a good overall behavior and the verification of the improvements.

Ai miei colleghi e amici
del "Laboratoire de l'Accélérateur Linéaire"

Contents

Introduction

The last decade in physics and astrophysics has drawn fundamental questions about the universe, its elementary particles, its forces and especially neutrinos mysteries. Because of their successes, which have led to a growing interest in the deep science, underground experiments will play a unique role in addressing these questions. Indeed, world wide scale international collaborations have already started their work on numerous future underground detectors. The trend toward internationalization accelerates with the increasing size and complexity of experiments.

The idea of the PMm² R&D program "Innovative electronics for photo-detectors array used in high energy physics and Astroparticles" has been conceived in 2005 at the Next generation of Nucleon and Neutrino detectors (NNN05) thanks to the collaboration with the Photonis Company and three French national laboratories. This project, considering the need of the future underground detectors to reach grand dimensions while reducing electronic complexity, has been proposed and accepted by the ANR in 2006. PMm2 stands for "square meter photomultiplier".

The first chapter of this thesis will give a detailed description of the PMm² program as well as a state of art of the Cerenkov detectors since they will be its main application.
The rest of this document will be dedicated to my contribution to this project which is the development of the front-end ASIC, PARISROC, and its characterization.
The ASIC realization requires a complete and rigorous path which is distinguished by different phases:

- The specification elaboration;
- The functional conception;
- The architecture conception;
- The design and realization;
- The measurements.

The first phase is based on the analysis of the project needs due to the physics and the detector structure that will be described in the first chapter.

The project requirements lead to the functional ASIC conception. In this second phase are defined the ASIC requirements and its architecture specifications which need a theoretical study supported by a large number of simulations. This phase terminates in a final ASIC structure conception. These two steps are described in the second chapter with a whole ASIC description.

The design and realization of the first ASIC prototype is followed by a phase of extensive measurements necessary to test the ASIC performances. The third chapter will describe the numerous measurements and the main results showing good agreement as well as few discrepancies with respect to the simulation.

The fourth chapter will describe the motivations of a second version of the ASIC and the new structure. The main simulation and measurements will be described to explain the modifications and to show the improvements with respect to the first version.

Chapter I

PMm² R&D Program

1. Introduction

The PMm² project [1] belongs to an R&D program funded by the French National Agency for Research (ANR)[1] with the complete title: "Innovative electronics for photo-detectors array used in high energy physics and Astroparticles". This R&D is carried out by three laboratories (LAL, IPN and LAPP)[2] and the Photonis[3] Company, a French photomultiplier tube manufacturer. In 2009 the ULB (Université Libre de Bruxelles) has joined the project to the DAQ developpement.
Photo-detection is a basic technique widely used in astroparticles and particles physics and the coverage of large areas of photo-detection is a crucial element of experiments studying high energy atmospheric cosmic showers and neutrinos from different sources (sun, atmospheric, supernova, reactor and accelerator).
The next generation of experiments such as MEMPHYS[4] and LENA[5] in Europe, Hyper-Kamiokande in Japan or LBNE[6] in USA could not base their programs only on a simple enlargement of existing experiments to improve the detection performance. Bigger detectors implicate a higher number of photomultipliers of large dimensions. Therefore the efforts of these new R&D programs have been concentrated on the complexity reduction[7]. In this international competition, the PMm² project has based its research on the development of a new generation "smart photo-detectors" which associate sensor and readout electronics. The project proposes to segment the large surface of photo-detection into macro pixels consisting of an array (2*2 m²) of 16 photomultipliers (PMTs) of 12-inches connected directly at their back to an autonomous front-end electronics which works in a triggerless data acquisition mode. The array is powered by a common high voltage and only one data cable for each one allows the connection by network to the central data event builder and filter. The PMm² project has concentrated its study on different subjects such as the front-end electronics (ASIC[8] and front-end card), the photomultipliers, the cables, the data transmission and the data acquisition (DAQ). In this chapter is described the PMm² program and the water Cerenkov detector which is one of its main applications.

[1] For three years exactly from 2007 to 2010 under the reference ANR-06-BLAN-0186.
[2] LAL (Laboratoire de l'Accélérateur Linéaire, Orsay, Université Paris 11); IPNO (L'institut de Physique Nucléaire d'Orsay Université Paris 11); LAPP(Le Laboratoire d'Annecy-le-Vieux de Physique des Particules, Université de Savoie).
[3] http://www.photonis.com/
[4] Megaton Mass Physics detector.
[5] Low Energy Neutrino Astronomy.
[6] Long Base line Neutrinos Experiment.
[7] This in turn is intended to induce the building and maintenances costs.
[8] Application Specific Integrated Circuit.

2. Physics motivations

The 30 year long tradition of large underground detectors has produced a rich number of discoveries. The pioneers were the water Cerenkov detectors (like IMB[9], Kamiokande[10]) that were built in the 80's to look for nucleon decay [2].
But their greatest achievement was that they have inaugurated:

- The study of astrophysics particles through the detection of neutrinos coming from the explosion of the supernova 1987 (Nobel Prize in physics in 2002 to Masatoshi Koshiba[11]);
- The study of neutrinos mass and neutrinos oscillation "observing" the atmospheric neutrinos and the solar neutrinos.

The scientific interest about these subjects has induced, in these last decades, number of experiments with different techniques such as water Cerenkov detectors with Super-Kamiokande or SNO[12] and scintillator detectors with BOREXINO[13] or KAMLAND[14].
Presently, the main aim of the research programs is to enlarge the discovery potential of these detectors on several domains to:

- Extend the proton decay sensitivity search;
- Have precise measurements of neutrinos oscillation parameters (i.e. masses, mixing angles) using different sources as solar, atmospheric, accelerator and reactor;
- Provide the study of the interior of a supernova explosion;
- Increase the understanding of the earth interior by the study of geoneutrinos;
- Detect neutrinos with high energy of astrophysical origin and also be sensitive to indirect decays of dark matter.

To reach this aim, the future proposed water Cerenkov detectors, belong to new R&D programs that develop an extension of mass to megaton scale of about a factor 20 more than Super-Kamiokande as for MEMPHYS, HyperKamiokande and LBNE. The rest of this chapter will be dedicated to these next generation water Cerenkov detectors and the connections with the PMm² program.

3. Cerenkov Detectors

Neutrinos are non-charged particles that have weak interactions with the matter. Therefore they can not be contained by classical detectors. The principle of their detection is then based on the fact that they can interact with the matter producing charged particles that can create Cerenkov light (see next sub-section) depending on the detector active material and their velocity.
Detectors with large quantity of water are used to enlarge the number of neutrino interactions with nucleons or electrons. These detectors are realized as large tanks filled with water and with the walls covered by photo-detectors to observe the light produced by the physics events. Their energy, direction, interaction point and the type of the charged particle are deduced by the information from the PMTs.
The detectors are located underground in order to reduce the background due to cosmic and atmospheric muons. Section 3.2 is dedicated to the description of the main water Cerenkov detector existing in the world: Super-Kamiokande (Figure 1.1).

[9] Irvine-Michigan-Brookhaven detector, Lake Erie-United States, 1979-1989.
[10] Kamioka Nucleon Decay Experiment, Kamioka Japan, 1986-1995.
[11] Japanese physicist that has been worked on the construction of the Kamiokande II detector.
[12] Sudbury Neutrino Observatory, Creighton Mine, Ontario, 1999-2006 (using heavy water).
[13] BORon EXperiment, Gran Sasso, Italy, 2007.
[14] KAMioka Liquid scintillator ANtineutrino Detector

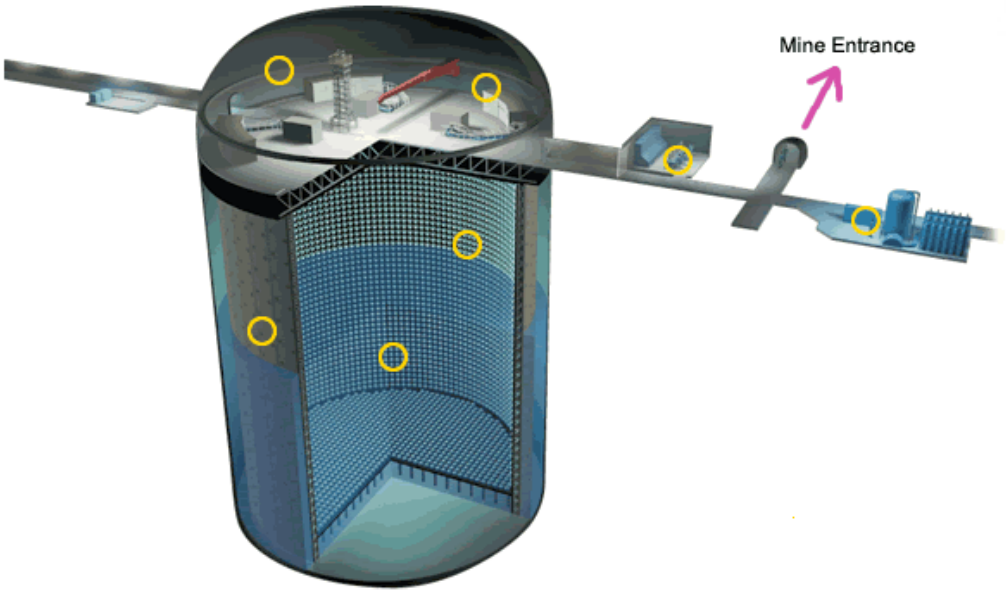

Figure 1.1. Schematic of the Super-Kamiokande water Cerenkov detector.

3.1. Cerenkov light

Cerenkov light is an electromagnetic wave which is emitted when a charged particle passes through a medium with a velocity faster than the light velocity in the medium as:

$$v \geq \frac{c}{n} \qquad (1.\ 1)$$

where v is the velocity of the charge particle, n is a refractive index of the medium and c is the light velocity in vacuum. The light is emitted in the forward direction of the traveling particle on a cone with an opening angle θ as (Figure 1.2)

$$\cos\vartheta = \frac{1}{n\beta} \qquad (1.\ 2)$$

where β is v/c. In water, n=1.33 – 1.36 therefore $\vartheta \cong 42°$ when β=1.

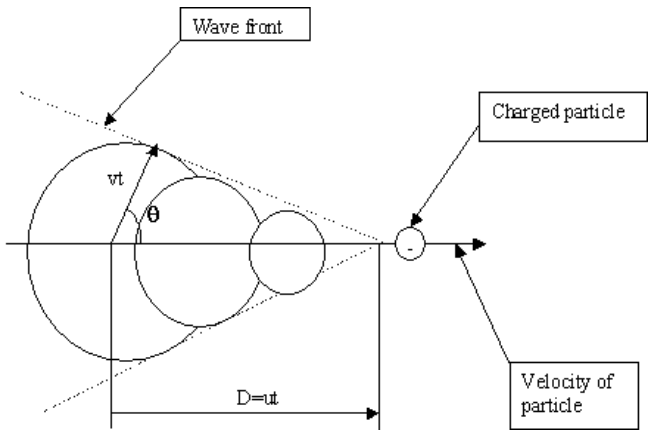

Figure 1.2. Cerenkov photon are emitted along the charge particle with an opening angle of $\theta=\cos^{-1}(1/n\,\beta)$ in water.

The number of Cerenkov photons, N, produced by a single charge particle per distance of propagation dx and wavelength dλ is given by:

$$\frac{d^2N}{dxd\lambda} = \frac{2\pi\alpha}{\lambda^2}\left(1 - \frac{1}{n^2\beta^2}\right) \qquad (1.\ 3)$$

Where α is the fine structure constant (~1/137). A particle with β=1 has a yield of 340 photons per cm in a wavelength range of 300-600 nm which is the photocathode efficient range of the photomultipliers use to collect this light. Figure 1.3 shows an example of the PMTs hit by the light that creates a ring shape.

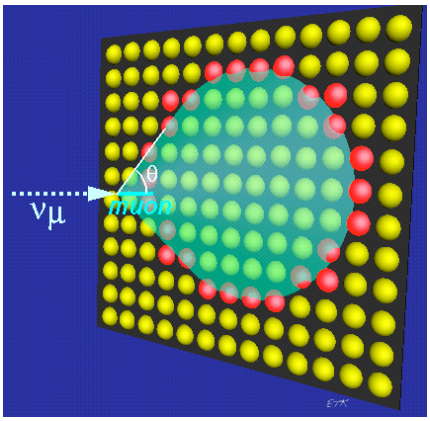

Figure 1.3. The Cerenkov photons, in a cone shape, which reach the photo-detectors (PMTs) that cover the walls.

3.2. Super-Kamiokande

The last detector version of the Kamioka Observatory (in Kamioka Town-ship, Japan) is Super-Kamiokande (Figure 1.4). It is the world's largest water Cherenkov detector since its commissioning in 1996. The detector cavity lies under the peak of Mt. Ikenoyama, with 1000 m of rock. It consists of a tank, 39 m diameter and 42 m tall, with total nominal water capacity of 50 kt [3].

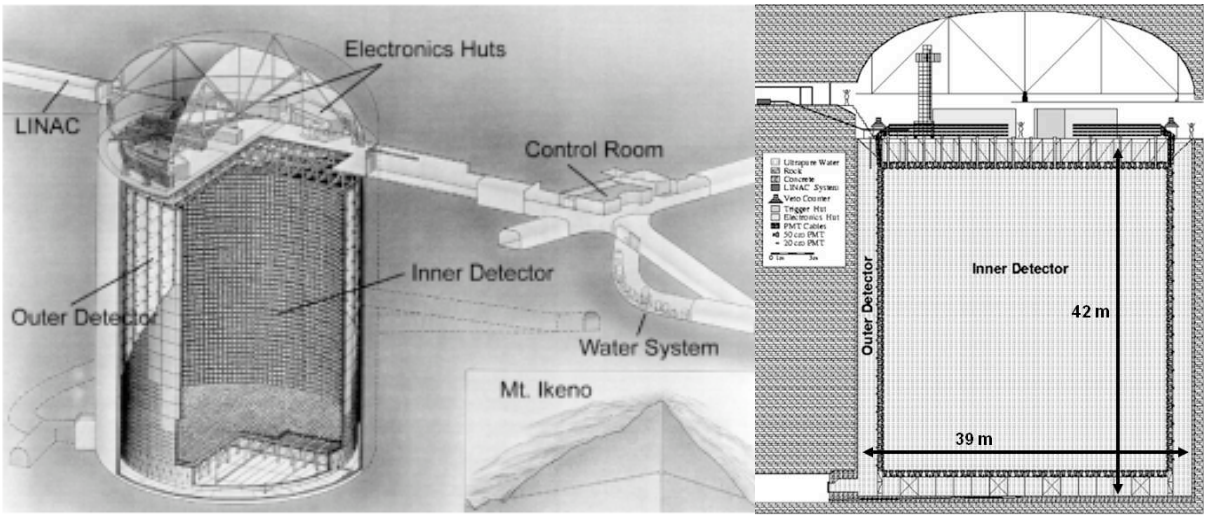

Figure 1.4. Left: Super-Kamiokande detector structure and on the right its cross-section.

The Inner Detector (ID) contains 32 kt of water and is viewed by 11146 inward-facing 20-inch PMTs that cover 40% of total surface area. The Outer Detector (OD) serves as an active veto counter against incoming particles (muons) and it is instrumented with 1885 outward-facing 8-inch PMTs. The two detector volumes are isolated from each other.

A 55 cm thick framework, located approximately 2-2.5 m from the tank walls on all sides, supports separate arrays of inward-facing and outward-facing PMTs. The framework is divided in modules of 4 * 3 20-inch PMTs in the bottom module and two 8-inch PMTs in the top module as illustrated in Figure 1.5.

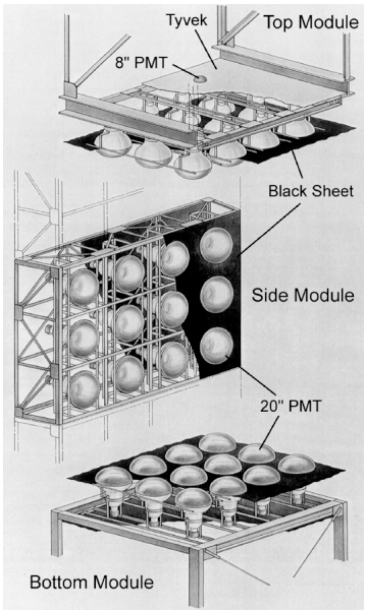

Figure 1.5. Schematic view of support structures for the inner detector.

The 20-inch PMTs characteristics are:

- The photo-cathode has peak quantum efficiency of about 21% at 360 – 400 nm;
- The collection efficiency for photoelectrons (p.e.) at the first dynode is over 70%;
- The transit time spread for 1 p.e. signal is 2.2 ns;
- The average dark noise rate at the 0.25 p.e. threshold is about 3 kHz[15];
- The ID PMTs were operated with gain of 10^7 at a supply high voltage ranging from 1700 to 2000 V;

Each PMT is connected to high voltage supplies and signal processing electronics via a single cable. These cables are all brought up to the tank top, where they are distributed to four "quadrant-huts" which contain electronics and front-end DAQ computers serving ID and OD PMTs for one quadrant of the detector.
Signals from 12 ID PMTs are sent to custom designed ATM (Analog-Timing-Modules) which provide arrival time and pulse area information with effectively low dead-time, due to a 2-channel ping–pong DAQ technique. The ATM has 450 pC of dynamic range (at PMT gain of 10^7 corresponds to 280 p.e.) with a resolution of 0.2 pC and 1300 ns of dynamic range in timing with a resolution of 0.4 ns.
The data collected by the server computers are transferred to the on-line host computer via network and merged to make complete events.
Super-Kamiokande can also take data continuously at 2.1 kHz triggering rate, which corresponds to 3.6 MeV total energy threshold with 50% efficiency.
Presently a new front-end electronics (2008) is implemented in Super-Kamiokande to improve the sensitivity of the detector for the following reasons [4]:

- Improve the dynamic range up to 2500 pC (PMT gain 10^7) for high energy neutrinos detection;
- Change the DAQ to record every hit of PMT (including dark current);
- Improve the speed for supernova bursts events (§ 6.3 Chapter I);

[15] At special conditions of temperature (13°) and free radon pure water.

The new front-end electronics is based on the module QBEE "QTC Based Electronics with Ethernet" made by a Time to Charge Converter (QTC) and a multi hit Time to Digital Converter (TDC). The timing resolution for single p.e. level signal is 0.3 ns, whereas the timing resolution of the 20-inch PMT signal is 2.8 ns for single p.e. level.
The trigger window of each AMT is of ~17 μs (TDC window). To record every hit continuously, the required speed is 1.5 MB/s per QBEE board which is equivalent to 10 kHz hit for every channels.

Figure 1.6 gives two events detected in Super-Kamiokande [5], on the left a muonic neutrino νμ interacting with a proton produces a muon that induces the Cerenkov light; on the right the Cerenkov light detected that has been produced by an electron.

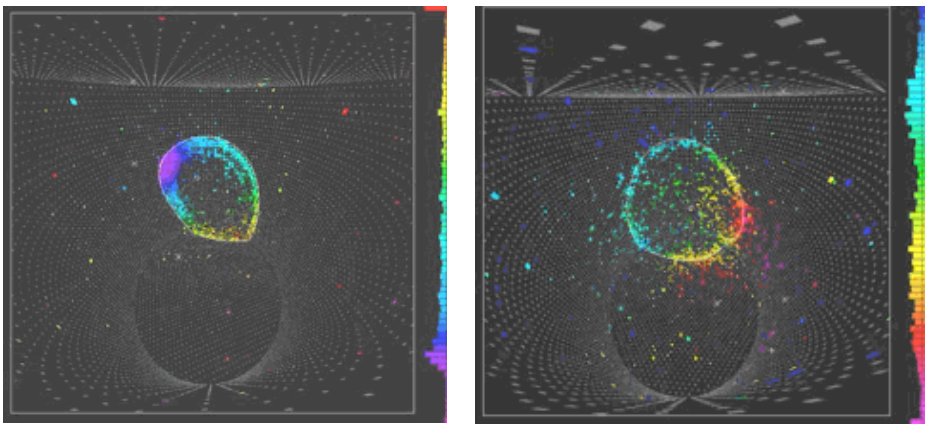

Figure 1.6. On the left muonic neutrinos ν_μ of 1063MeV that have an interaction with a free proton with the production of a muon of 1032 MeV. The muon produces Cerenkov light. On the right a 600 MeV electron; the ring is more diffused compared to the muon one.

The main physics events observed in water Cerenkov detector such as Super-Kamiokande are:

- The "solar neutrinos" and "reactor neutrinos" with low energy below 10 MeV;
- Neutrinos background from past Supernova explosion below 30 MeV;
- Neutrinos from "present" Supernova bursts that give a flux of $5*10^5$ events/Mt of 15 MeV in 10 s and half of them in 1 or 2 seconds.
- The "atmospheric neutrinos" and "accelerator neutrinos" with high energy levels from typically 1 to 20 GeV;

4. New generation water Cerenkov detectors

The 15 year long successful operation of the Super-Kamiokande detector has clearly demonstrated the capabilities and limitations of large water Cerenkov detectors [6]:

- A technique that is reliable and stable. However in order to instrument megaton scale detectors, significant cost is reached mainly due to the photo-detectors and their associated electronics (apart from the excavation cost of large cavities). Indeed the cost grows with the outer surface of the detector, while the active mass, made of water, is essentially free except for the purification system.
- The detectors size that is limited by different parameters: the finite attenuation length of Cerenkov light, found to be 80 m at λ=400 nm in Super-Kamiokande; the pressure of water on the photomultipliers at the bottom of the tank, which gives a practical limit of 80 m in height.
- The detection principle in measuring Cerenkov light has several consequences:
  - Neutral and charged particles below the Cerenkov threshold are undetectable, so that some energy can be missing;

- The threshold in particle energy depends on photocathode coverage and on water purity. Example: Super-Kamiokande has achieved an energy threshold of 4.5 MeV [7] with 40% cathode coverage.

Despite these limitations, considering alternative solutions using photo-detectors as the Liquid scintillators, it has been shown that the future large water Cerenkov detectors are competitive [8] and the physics that are addressed are[16]:

- Nucleon decay[17];
- Long baseline oscillation experiments[18];
- Solar neutrinos;
- Atmospheric neutrinos;
- Supernova neutrinos.

A Summary of the physics potential of two proposed detectors for astroparticle physics topics is shown on Table 1.1; the number of events attended for two detector techniques respectively the liquid scintillator LENA and the Cerenkov MEMPHYS are listed for the different physics topics.

Topics	LENA 50 kton	MEMPHYS 440 kton
Proton decay		
$e^+\pi_0$		$1 * 10^{35}$
$\bar{\nu}K^+$	$0.4 * 10^{35}$	$0.2 * 10^{35}$
Supernova ν (10 kpc)		
CC	$9 * 10^3$ (ν_e)	$2 * 10^5$
Supernova ν diffusion (S/B 5 years)	9-110/7	43-109/47
Solar ν		
^{8}B ES	$1.6 * 10^4$	$1.1 * 10^5$
Atmospheric ν (Evts. 1 year)		$4 * 10^4$
Geo ν (Evts. 1 year)	~1000	
Reactor ν (Evts. 1 year)	$1.7 * 10^4$	$6 * 10^4$

Table 1.1. Summary of the physics potential of two proposed detectors for astroparticle physics topics. The columns list the number of events attended for respectively the liquid scintillator detector Lena and the water Cerenkov detector Memphys [8].

Three similar water Cerenkov projects are being carried out worldwide: Hyper-Kamiokande in Japan, MEMPHYS in Europe and LBNE in USA.

4.1. The detectors design

The future Cerenkov detectors will reach a fiducial mass around half a megaton. The main difference between the projects lies in the geometry of the cavities (tunnel shape for Hyper-Kamiokande, shafts for MEMPHYS and for LBNE).
One of the Japanese Hyper-Kamiokande designs [10] is based on two twin tunnels with 2 * 275 kt of fiducial mass and dimensions: 54 m of height, 48 m of width and 250 m of total length (Figure 1.7). The two twins contain 5 optically independent cylindrical compartments.

[16] Alternative is 100 kt liquid Argon TPC (Time Projection Chamber) that gives also sensitive measurements.
[17] Essentially through $p \rightarrow e^+ \pi^\circ$ although other channels are studied [9].
[18] From CERN to MEMPHYS and from Fermilab to LNBE.

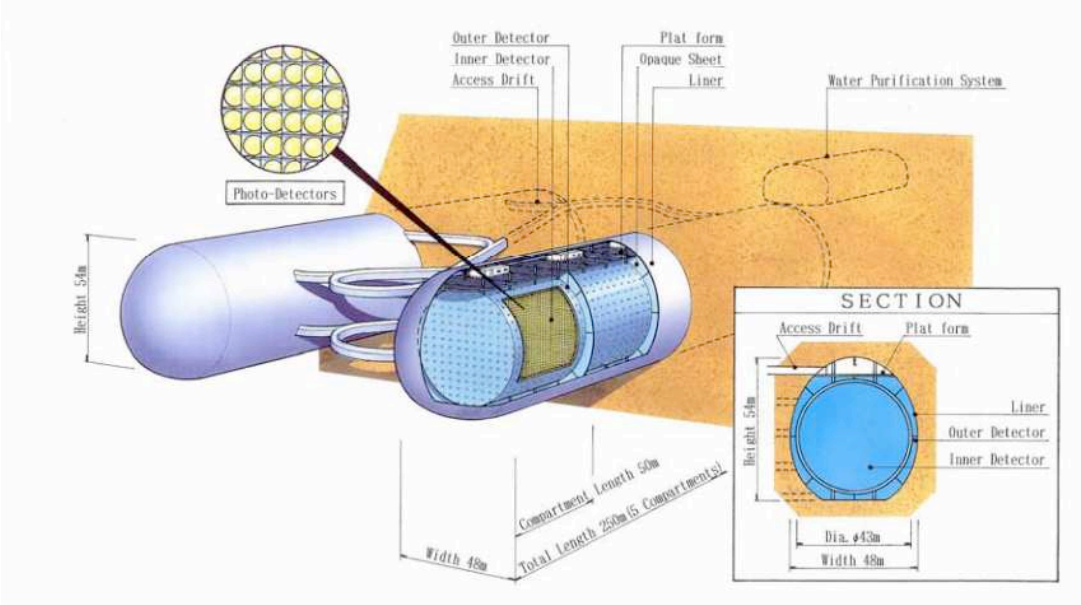

Figure 1.7. Hyper-Kamiokande detector will be based on two twin tunnels with 0.550 Mt of fiducial mass and dimensions: 54m of height, 48m of width and 250m of total length.

The European project, MEMPHYS, [6] (Figure 1.8) will be based on 3 shafts[19] each with 65 m of diameter and 65 m of height for the total water container dimensions to reach the 440 kt of fiducial mass.

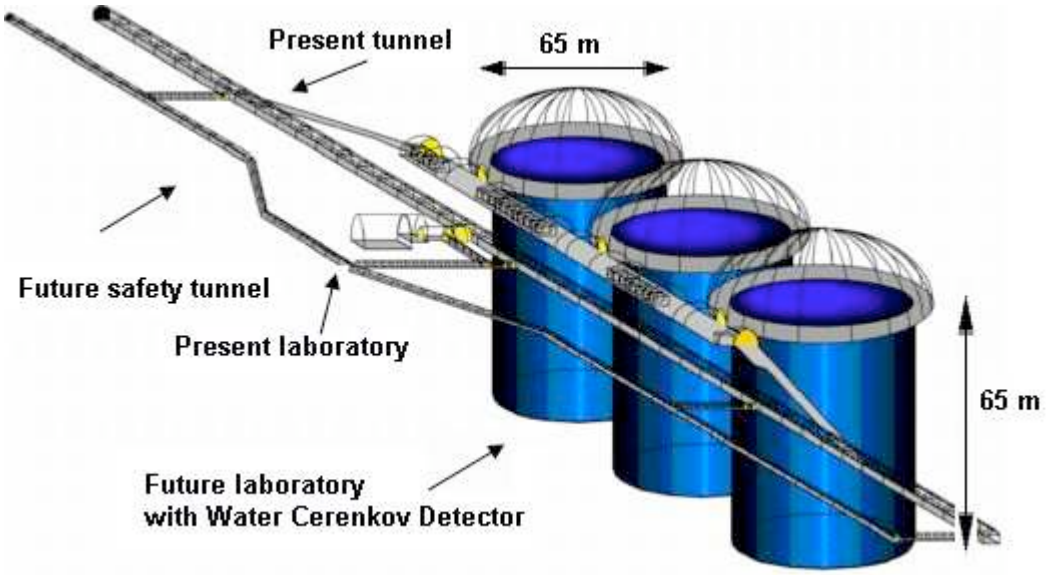

Figure 1.8. Memphys detector will be based on 3 shafts each with 65 m of diameter and 65 m of height for the total water container dimensions to reach the 440 kt of fiducial mass.

The LBNE project [11] (Figure 1.9) is based on the water Cerenkov detector, very similar to the MEMPHYS design, with 3 cylinders of 53 m diameter and 60 m height.

[19] Up to 5 shafts are possible.

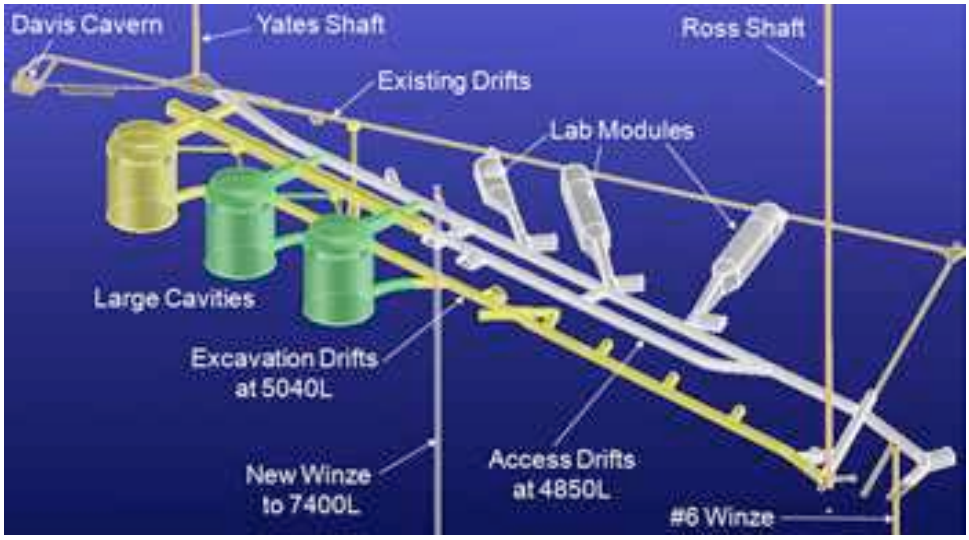

Figure 1.9. The envisioned Water Cerenkov detector for LBNE project is made by 3 cylinders of 53 m diameter and 60 m height.

4.2. Location

An important parameter for the three detectors is the cavities location and the rock overburden. The Hyper-Kamiokande detector [10] will be located in underground laboratories at around 1500 m.e.w (meter equivalent water) and the better site is under investigation. Two possibilities are studied: the Tochibora and Mozumi mines. A preliminary study of the candidates has brought, for the rock properties, to the Toshibora mine (Figure 1.10).

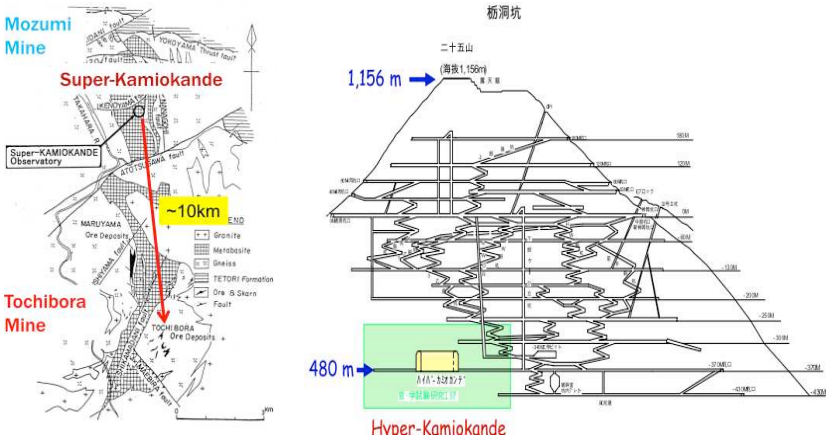

Figure 1.10. The detector will be located in underground laboratories and two possibilities are studied: the Tochibora mine and Mozumi mine. On the left the general project map and on the right the Tochibora mine scheme.

The MEMPHYS project belongs, with other two options GLACIER[20] and LENA, to a more general program named LAGUNA[21] that is a European project carrying on underground sites studies and developments in view of such detectors observatories [12]. The program is evaluating possible locations of the underground laboratories and in Table 1.2 are summarized some basic characteristics of the sites under consideration, including the distance from CERN, which is relevant in case a neutrino beam is sent from CERN to the selected underground site.

[20] Giant Liquid Argon Charge Imaging ExpeRiment.

[21] Large Apparatus studying Grand Unification and neutrinos Astrophysics.

Location	Type	Envisaged depth m.e.w.	Distance from CERN (km)
Fréjus (F)	Road tunnel	~ 4800	130
Canfranc (ES)	Road tunnel	~ 2100	630
Umbria (IT)	Green field	~ 1500	665
Sieroszowice (PL)	Mine	~ 2400	950
Boulby (UK)	Mine	~ 2800	1050
Slanic (RO)	Salt Mine	~ 600	1570
Pyhasalmi (FI)	Mine	Up to ~ 4000	2300

Table 1.2. LAGUNA basic characteristics of the sites under consideration.

The LNBE detectors could be housed in the proposed deep underground science and engineering laboratory in South Dakota DUSEL (at Homestake) [11] (Figure 1.11) and the caverns would be located ~1400 m underground.

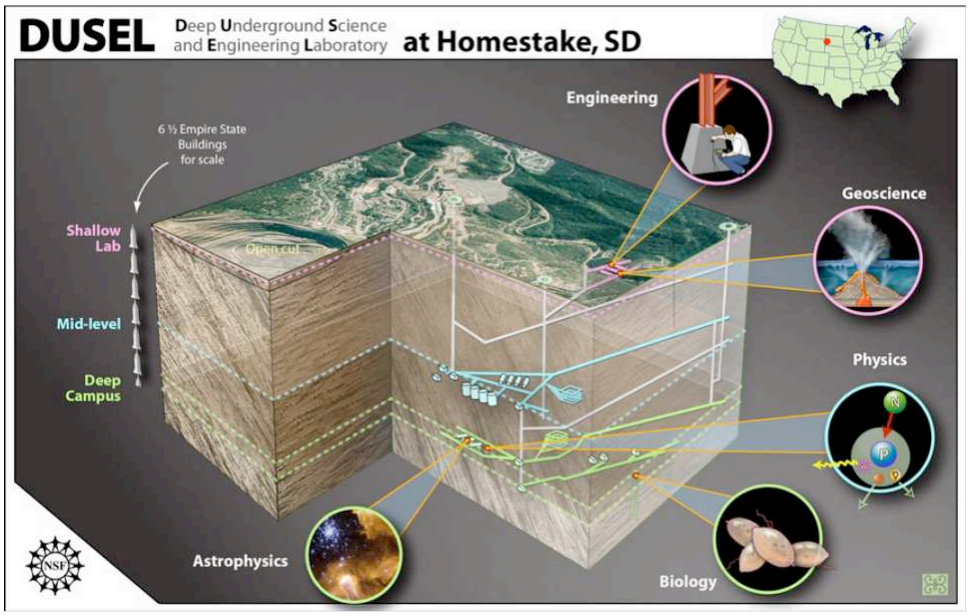

Figure 1.11.The LNBE detectors could be housed in the proposed Deep Underground Science and Engineering Laboratory in South Dakota DUSEL (at Homestake).

4.3. Photo-detection

The choice of the photo-detectors for the three detectors is mainly focused on the photomultiplier, successfully used in the previous generation of large Cerenkov detectors. The PMT density should be chosen to allow the better sensitivity with a compromise with the costs.

The Hyper-Kamiokande project is studying different possibilities to cover the two twins: by using 100000 or 200000 20-inch PMTs with photo coverage of the 20-40 % of the entire surface[22] or by using a new generation of HAPD (Hybrid Avalanche Photo-Detector) [10].
The 20 inch-PMTs are expensive as these tubes are manually blown by specially trained people, so in producing 100000 units the costs would become elevated to which should be added the cost of the associated electronics (one for each PMT). The R&D programs are thus concentrated on the reduction of the cost problems with [13]:

- Smaller number of detectors with better performances in quantum efficiency (QE);

[22] It has been shown after the SuperKamiokande accident that some physics events have comparable sensitivity with reduced surface coverage (eg. accelerator neutrinos and proton decay into $e^+\pi^0$) [9].

- Cheaper detectors;
- Cheaper electronics.

A study of the photocathode material is in progress to improve the QE for the HAMAMATSU PMTs as well as a research on large HPDs in Japan (Figure 1.12) driven mainly by the need to get lower prices than the present 20-inch PMTs. This research has brought encouraging results such as photoelectron sensitivity, wide dynamic range, good timing and good noise to signal separation. These HPDs need to be operated at 20 kV high voltage and low noise fast electronics.

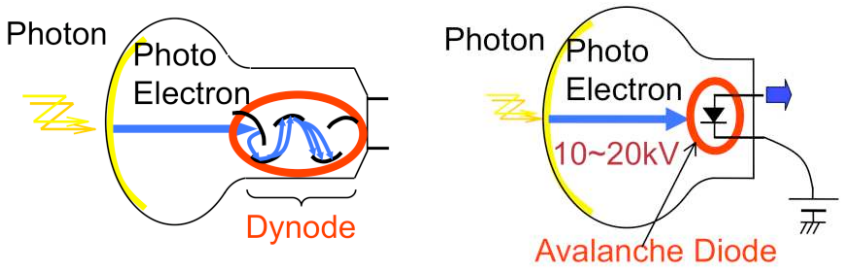

Figure 1.12. PMT and HPD general schematics.

In the MEMPHYS design, the inner detector is covered by about 81000 12-inch PMTs to reach a 30% surface coverage. The fiducial volume is defined by an additional conservative guard of 2 m (veto mass). The outer volume between the PMT surface and the water vessel is instrumented with 8-inch PMTs.
The LNBE project is similar to MEMPHYS with little differences such as the number of large PMTs used which is around 50000-100000.
The use of 12-inch PMTs has been motivated by PHOTONIS Company [14] with respect to the 20-inch, for the following reasons (see Table 1.3):

- They can be automatically manufactured therefore are cheaper;
- They have better QE and time collection efficiency (CE);
- Faster rise time;
- Smaller jitter.

PHOTONIS had estimated that the price per useful photoelectron of the 12-inch would be 1.6 lower than the 20-inch one (Table 1.3). With these characteristics the 30% coverage with 12-inch PMTs would give the same number of p.e. per MeV as the 40% of coverage with 20-inch one.
Despite the benefit to use 12-inch PMTs, after the halt of PHOTONIS Company PMT researches and developments, the cost scenario should be revisited with the development strategy of the HAMAMATSU Company.

Diameter (inches)	20	17	12
Projected area (cm²)	1660	1450	615
Quantum efficiency (typ) (%)	20	20	24
Collection efficiency (%)	60	60	70
Cost (€)	2500	2500	800
Cost/(cm² x QE x CE)	12.5	14.4	7.7

Table 1.3. PMTs characteristics [14].

A summary of the different projects is shown on Table 1.4; numbers for LENA experiment are also given for comparison.

	Type of detector	# PMTs/module	Fiducial mass
Hyper-Kamiokande	Water Cerenkov	100000	~ 500 kt
Memphys	Water Cerenkov	81000	~ 500 kt
LBNE	Water Cerenkov	50000	~ 300 kt
LENA	Liquid scintillator	13000	~ 50 kt

Table 1.4. Summary of the future detectors characteristics in terms of number of PMTs and fiducial mass.

5. PMm² program

5.1. General description

Along the line of the world wide R&D effort, the PMm² has investigated an alternative option to the realization of large detectors with vast numbers of PMTs, developing a new generation of "smart photo-detectors" which associate sensors and readout electronics.
The program has proposed to segment the large surface of photo-detection[23] in macro-arrays of (2*2 m²) realized with 16 PMTs of 12 inches (Figure 1.13).

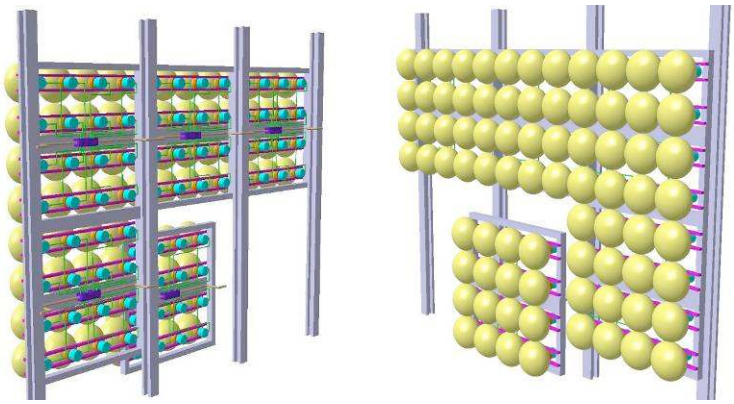

*Figure 1.13. The macro-arrays of (2*2 m²) realized with 16 PMTs of 12-inches.*

Each array is connected to an innovative autonomous electronics system located closed to the PMTs that can implement different functionalities including the digitization of the data.
The progresses in microelectronics allow to integrate several channels in the same ASIC and implement several elements, from amplification up to digital conversion. The ASIC provides exclusively the broadcast of the digital data via an Ethernet network to an online data acquisition system. The use of this ASIC provides increased reliability and decreased per-channel cost.
The 16 PMTs in the array are supplied with a common high voltage bias, distributed by the front-end module, and a single data cable for each array for the communication with the surface card (Figure 1.14).

[23] 20,000 m² envisaged for one tank of MEMPHYS (see section 4.1 Chapter I).

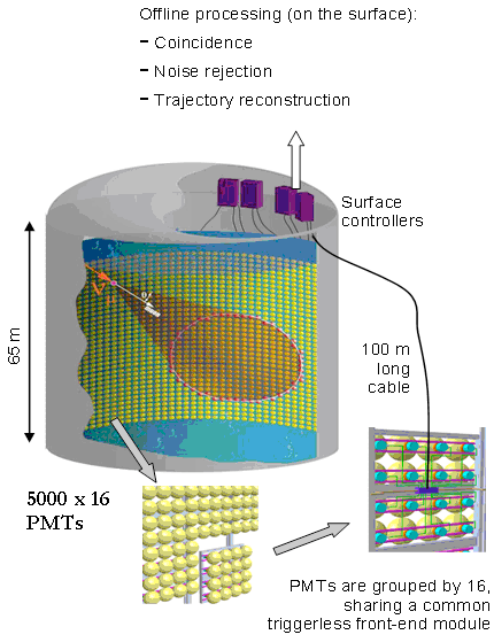

Figure 1.14. Principle of PMm2 proposal for megaton scale Cerenkov water tank with ~5000 arrays of 16 PMTs shown in the bottom side of the picture. Are emphasized the surface controller and the 100 m of cable.

The PMm² program has concentrated its research on few subjects (Figure 1.15) such as the development of the front-end electronics (ASIC and front-end card), the improvement of the 12-inch photomultipliers[24], the cables, the data transmission and the DAQ.

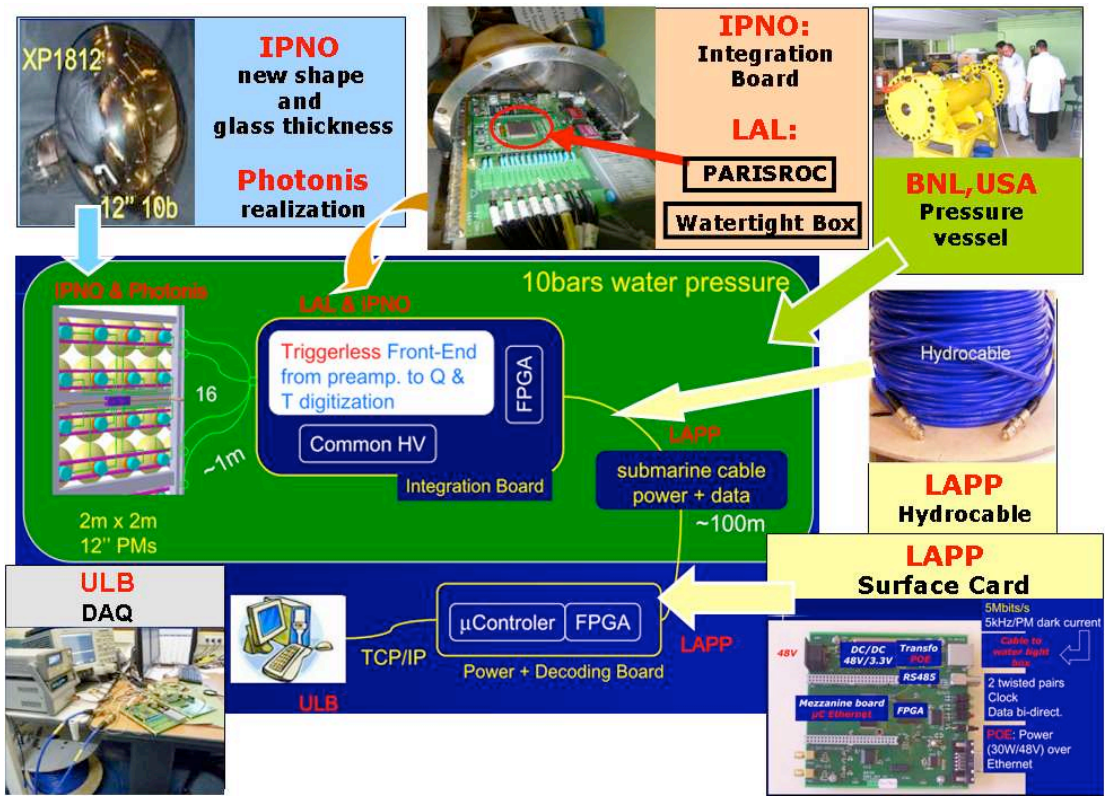

Figure 1.15. General structure of PMm² project.

[24] Originally from the PHOTONIS Company, but after the halt of their PMT research department, the use of 8-inch HAMAMATSU PMTs has been chosen to build a demonstrator test module.

5.2. The front-end electronics

The PMm² program is mainly addressed to the water Cerenkov detectors, explained in § 3 Chapter I, but is applicable to all the detectors realized with a large number of PMTs. As described in § 3.2 Chapter I, in the Super-Kamiokande detector the PMTs are located on the walls of the tank thanks to a framework divided in module of (4*3) 20-inch PMTs, each PMT is connected to high voltage supplies and signal processing electronics via a single cable that is brought up to the tank top where the front-end electronics is located. The PMm² program, using the same concept, proposes to group 16 PMTs in an array, as shown on Figure 1.16, connected to a common front-end electronics placed in an enclosure, located underwater, close to the PMTs.

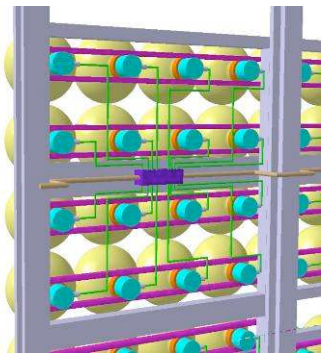

Figure 1.16. Array of 16 PMTs, connected to a common front-end electronics located in an enclosure underwater close to the PMTs.

As the front-end ASIC (PARISROC) developed by LAL-Omega team is the main subject of this thesis the design and measurements are described extensively in chapters II and III. The other components of the front-end electronic will be summarized in the following sections.

The front-end card (Figure 1.17), studied and realized by the IPNO, has to achieve the PMTs bias, the slow control, the data digitization and the interface with the cable connection to the surface. It has two main components: the PARISROC and the FPGA (Altera Cyclone 3). The card is supplied by 48 V through a Power Over Ethernet Plus (POE+) technology and submarine cable. Then a series of DC/DC converters supply the voltage levels necessary for the board, the ASIC and the high voltage (up to 2 kV) to bias the 16 PMTs.
The FPGA is used as a link between PARISROC and the surface controller, managing the slow control commands and the output data flow. The front-end card is connected to the surface by 100 m of submarine cable, studied by the LAPP[25], made of three differential pairs: one is used to receive the unidirectional 10 MHz clock, one is bidirectional for the data with POE feature and the last one is not used. The use of a single twisted pair has not been investigated for simplicity although the IceCube collaboration [15] has shown that both the data and the power can share the same pair. This point is not a critical issue and is left for future developments.

[25] In collaboration with Hydrocable and Euroceanique companies.

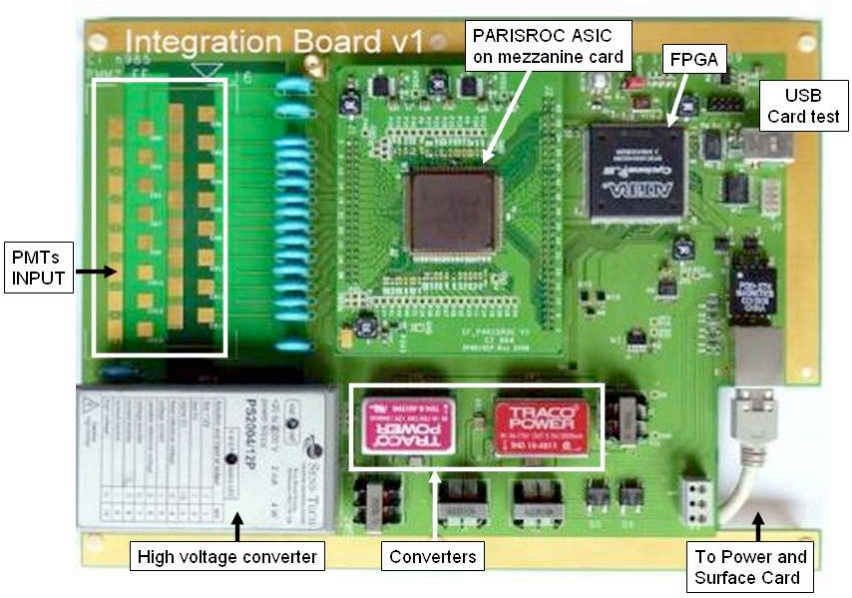

Figure 1.17. The front-end card. Main components: ASIC and FPGA.

A waterproof enclosure has been realized by the LAL[26] to place the front-end under water and is shown on Figure 1.18.

Figure 1.18. The waterproof enclosure realized to place the front-end under water.

5.3. 12-inch PMT

The specifications on the PMTs are governed by the physics requirements and the immersion in a deep water volume. Considering the specific case of MEMPHYS detector (§ 4.1 Chapter I), it is considered that the PMT should resist up to 10 bars, even if a specific envelop has to be designed to manage the impact of a PMT implosion that would produce a shock wave of about 50 bars to its close neighbors [16]. Mechanical simulations have been performed and then validated by measurements by IPNO on PMTs

[26] At the "Service de développements et de technologies mécaniques".

with a diameter ranging from 1.5 to 12 inches (left of Figure 1.19) equipped with strain gauges in a pressure vessel[27] certified up to 150 bars and shown on the right of Figure 1.19.

Figure 1.19. Left: the 12-inch PMT equipped with strain gauges and PMT with broken glass because of the pressure. Right: the vessel for the pressure tests shipped from BNL laboratory.

The mechanical design has been computed by IPNO mechanical department using the CATIA software and then Photonis Company has designed the electrostatic part and has produced the glass envelop to build fully equipped PMT prototypes. This kind of reinforced PMT, especially at the foot, has succeeded to resist up to 20 bars. Unfortunately, the Photonis Company has closed all the production of the PMTs in 2009 therefore all the measurements with the front-end electronics are made with different PMTs: PHOTONIS 1-inch and 10-inch (§ 9.5 Chapter III) and finally with HAMAMATSU 8-inch PMTs.

5.4. Surface Card

The surface card, studied and realized by the LAPP, has been conceived to manage the power supply, the communication and the synchronization with the watertight box immersed in the water. The digitized data are transmitted, over 100 m of submarine cable, to the surface card with a dedicated serial protocol at a rate of 5 Mbps (possible up to 10 Mbps) that was determined assuming that the noise for a single PMT is 5 kHz[28], and that there are 52 bits of data per PMT. The main data rate is produced by the dark noise of the PMTs as there is no local coincidence trigger at the level of 16 PMTs array. The rate of 5 kHz/PMT implicates therefore a total 80 kHz rate per the array with 4 Mbps of data.
In a detector, as MEMPHYS, the DAQ will manage 5000 independent arrays which correspond to a data stream of 25 Gbps. In comparison the new Super-Kamiokande software, the design of the data flow is about 7 Gbps [18].
The surface card is designed with a FPGA which manages the communication and the synchronization with the watertight box and a microcontroller which insures the communication with Ethernet network to a PC using JAVA software in order to analyze incoming data. The card transmits a 10 MHz clock synchronized by GPS to the front-end ASIC to assure the time measurements in each array of PMTs and to synchronize these measurements among the different arrays.
The surface card and the cable are displayed in Figure 1.20.

[27] The vessel is loaned to IPN Orsay by the Brookhaven National Laboratory thanks to BNL-IPNO partnership.

[28] Estimated value by extrapolation of various measurements on different PMT dimensions (Photonis) in function of the temperature [17].

Figure 1.20. The surface card and an example of the cable and watertight connector.

6. ASIC requirements coming from physics motivations

As seen previously (§ 4 Chapter I), the physics subjects of the next generation of large detectors are different in terms of energy and number of events reached per time unit. Cerenkov light provides photons detected by photo-detectors (PMTs) which cover the walls.
The detector purpose is the reconstruction of the parameters of the primary particle:

- The type of the particles;
- The direction;
- The energy.

The type of particle is deduced from the shape of the Cerenkov light ring produced which is directly linked to the charge distribution over the total number PMTs.
The particle direction is obtained by the time of flight of the Cerenkov photon (the time measurements). The time and charge measurements allow the reconstruction of the event vertex i.e. the particle point of interaction. These are measured by the electronic front-end and then treated by sophisticated software.
This section will explain the ASIC requirements determined by:

- The main physics events treated by the detectors;
- The detector structure (dimension, water, PMTs, etc).

6.1. Trigger threshold and dynamic range

The Cerenkov light during its propagation in the water, before reaching the PMTs, is attenuated, due to a combination of scattering and absorption of the intensity of the light. Moreover the detector surface (the walls of the tank) is not completely covered by the photo-detectors. As a reminder the Super-Kamiokande detector has 40% of its total surface used to detect the light.
Therefore the number of photons that reach the PMTs depends of:

- The type of the charged particle;
- The charged particle flight distance;
- The water absorption and diffusion;
- The PMT coverage and its quantum efficiency.

For example for an electron interaction in the water, the estimation gives a production of 8 p.e./MeV and 1.5 p.e./MeV for a muon (Super-Kamiokande results). Considering the expected energy of the charged particles, a small number of p.e. will be produced and observed in the detector. Therefore in most of the cases only one Cerenkov photon will be detected by a single PMT. This means that the electronic front-end must be efficient at 1 p.e detection in order to reconstruct accurately the event.
The PMT ability to detect 1 p.e. depends also on the PMT noise: a noise signal of 1 p.e. cannot be distinguished from the real signal.
The Super-Kamiokande PMTs noise rate is of 3 kHz with threshold of ¼ of p.e [3] in fresh radon free ultra pure water. The design goal of PMm[2] is to manage a PMT dark rate of about 5 kHz with a threshold of 1/3 of p.e. This is a conservative number as in principle the dark rate scales according to the photocathode surface everything else kept constant.

Figure 1.21 and Figure 1.22 show data collected by the Super-Kamiokande detector without any cuts. In the first the distribution is represented of the total number of p.e. collected in a time window of 300 ns, and in the second the ratio of the number of p.e collected by a single PMT over the total number of p.e collected by the whole set of PMTs. From this distribution it can be argued that the maximum number of p.e collected per event is of order 10^6 and these p.e. are shared among all the PMTs of the event, so one PMT collects a maximum of about 100 p.e. Notice that due to multiple reflections on the glass PMT surfaces and wall surfaces, the number of PMTs hit per event in a 300 ns time window is a large fraction of the total number of PMTs.

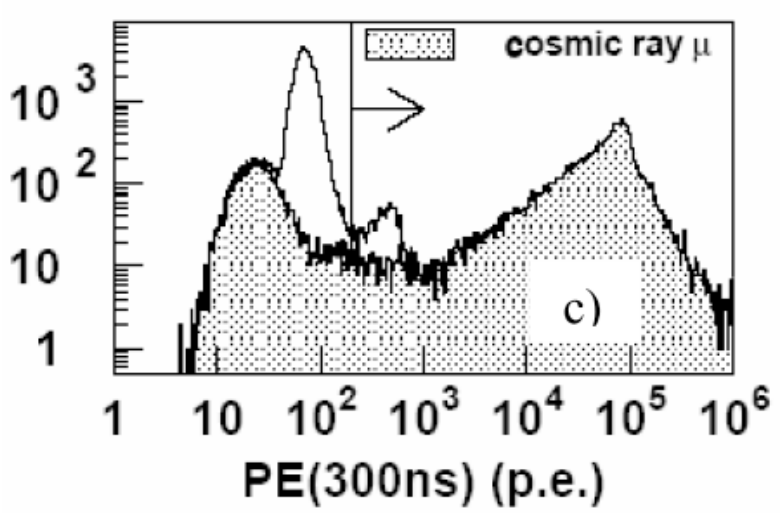

Figure 1.21. Super-Kamiokande raw data collected during 535 days during phase I [19]. It is displayed the total number of p.e. in a time window of 300 ns on the totality of the PMTs (11.000). As it is explained in the reference, the cosmic ray muons giving hits in the outer detector are shown on the hashed histogram. Beyond this large contribution, the first peak at ~60 p.e corresponds to low energy radioactivity, while the peak at ~500 p.e corresponds to electrons produced by muon decays.

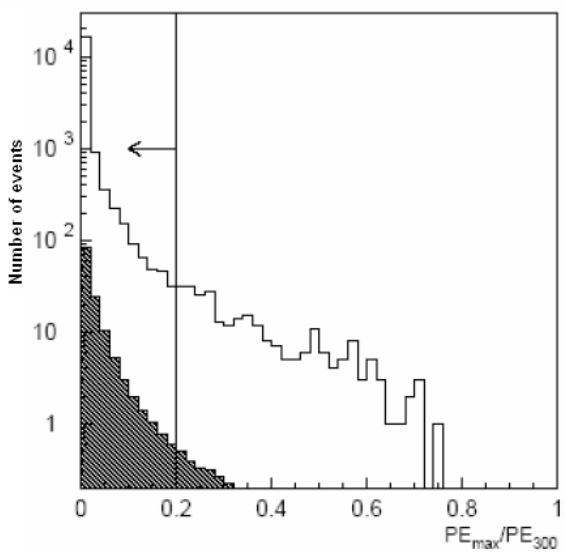

Figure 1.22. The distribution of the p.e. detected by a single PMT (PE_{max}) comparing to the totality of p.e. detected in a time window of 300 ns (PE_{300}) [19].

Simulations for the MEMPHYS project have been done[29] [1] to confirm these numbers in a new setup. As an example let us look at results using atmospheric neutrino events that are described in the following.

- **Atmospheric neutrinos events**

The number of p.e. per PMT are simulated for 1000 atmospheric neutrinos events with energy between 1 and 10 GeV in a cylindrical volume of water of fiducial mass of 160 kt.
The time distribution of the photon arrival times detected in these kinds of events is displayed in Figure 1.23. The time zero for each event is the time of interaction of the primary neutrinos. The distribution is driven by the multiple reflections of the Cerenkov photons onto the PMT glasses and the walls even if the later are covered by black sheets. The "gas" of photons decreases by the absorption mechanism which acts as leakage. This explains the exponential behavior with a mean value around 150 ns and an rms value of 116 ns.

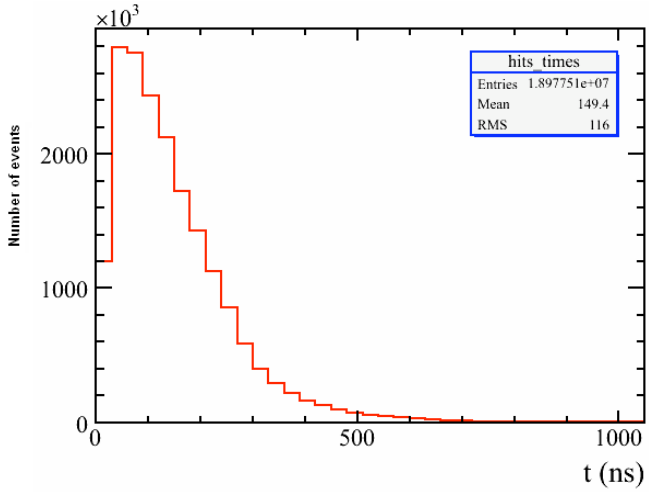

Figure 1.23. The time distribution of the photon arrival times for simulated 1000 neutrinos atmospheric events.

[29] J.E. Campagne simulations (PMm² Project Leader) with Geant4.

The atmospheric neutrinos' total energy distribution is displayed on Figure 1.24 and a mean value of 3 GeV has been obtained.

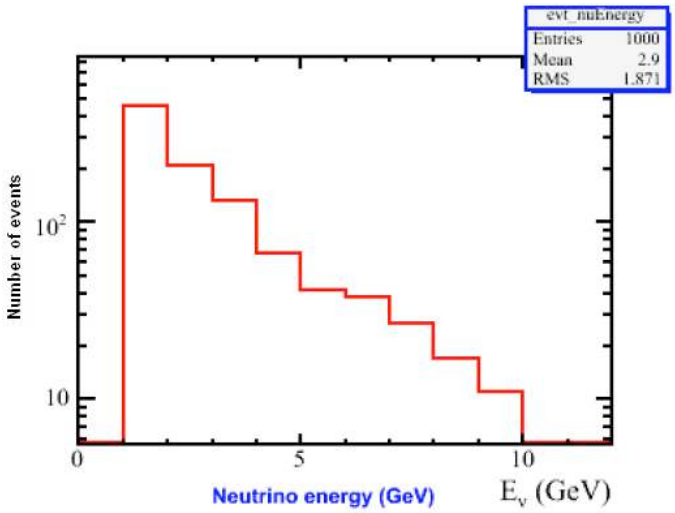

Figure 1.24. The atmospheric neutrinos total energy distribution for simulated 1000 neutrinos atmospheric events.

For such neutrinos, the fraction of PMTs hit in one event is around 10% and the distribution is indicated in Figure 1.25.

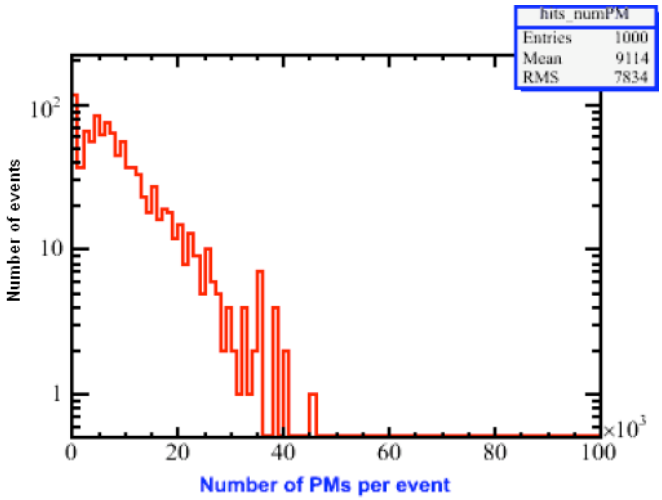

Figure 1.25. Distribution of the number of PMTs hit obtained from simulated neutrino atmospheric events.

The distribution of the number of p.e. detected by each PMT is shown in Figure 1.26 which exhibits an exponential behavior pointing out the necessity to trigger efficiently on single p.e. It is also shown that the maximum number of p.e registered by a single PMT is a few hundred of p.e.

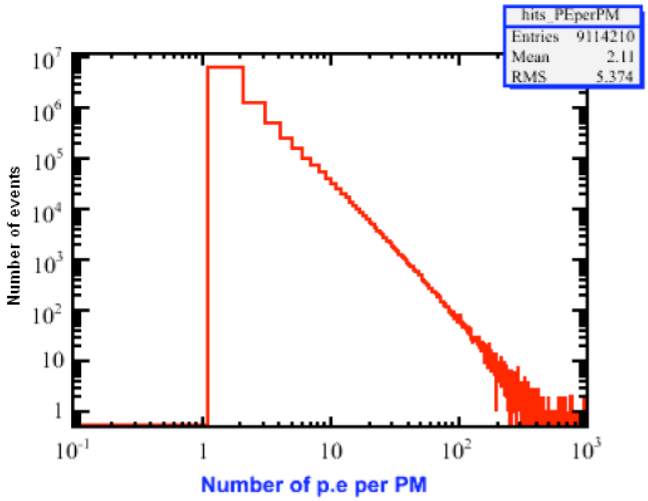

Figure 1.26. The distribution of the number of p.e. detected by each PMT for 1000 simulated neutrinos atmospheric events.

Figure 1.27 shows the number of PMTs that have detected a number of p.e. bigger than 300 p.e. This simulation indicates that 90% of the events have a p.e. production less than 300 p.e. and, in the remaining 10%, only 1% of the total number of PMTs have detected a number of p.e. greater than 300 pe.

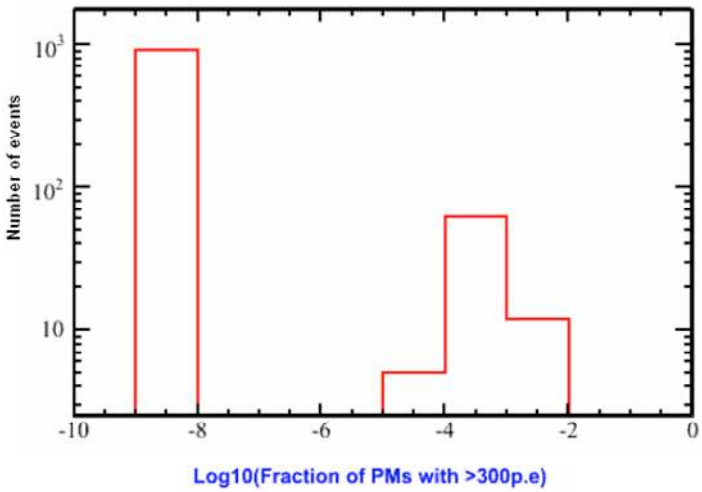

Figure 1.27. The number of PMTs that have detected a number of p.e. bigger than 300 p.e. for 1000 simulated neutrinos atmospheric events.

The requirements for the front-end ASIC motivated by the above simulations and Super-Kamiokande operation is then to trigger 100% at 1/3 p.e. and to reach a dynamic range of 300 p.e.

6.2. Time requirements

The relative time of PMT hits is important for event reconstruction: a good time measurement is necessary for an accurate vertex reconstruction using the time of flight, which has a direct impact on the fiducial volume determination and indirect impact of the electron/muon identification through the "ring" morphology analysis.

It has not been possible to perform an analysis of the impact of time resolution on event reconstruction in the context of MEMPHYS detector due to the lack of relevant software. So, as a pragmatic approach we have fixed the same requirement as for the Super-Kamiokande detector, that is to say to be able to

perform 1 ns time-tagging. Moreover, for large PMTs the time spread is of this order of magnitude so it would be hard to perform sub-nanosecond measurements.

6.3. Dead Time

Theoretical calculations of supernova explosions suggest that neutrinos are emitted over a total time-scale of a few tens of seconds with about a half of them emitted during the first second.
About 10000 total events are expected in Super-Kamiokande for a supernova explosion at the center of our Galaxy. Super-Kamiokande can measure a burst with no dead-time, up to 30000 events in the first seconds of a burst.
The performance of the system for supernova detection can only be estimated by the measurement of dead time with simulated high-rate event bursts. In the Table 1.5 are listed the performances obtained at Super-Kamiokande with the first generation electronics.

Trigger rate (kHz)	Total number of events	Dead time (%)
7.5	50000	0
21	150000	14
45	300000	32
75	500000	60

Table 1.5. The dead time performance with the Super-Kamiokande first generation electronics [3].

In case of a supernova explosion at 4 kpc (kiloparsec) from Earth, in Super-Kamiokande it is expected 60000 events for 20 kT fiducial mass during 10 s. So Table 1.5 indicates that these events would be stored practically without any dead time. Although with a new electronic design, mainly due to triggerless mode [4] and software filtering, it has been shown that a rate of 130 kHz can be achieved without dead time. This corresponds of about 1 kpc supernova burst signal.

For the next generation of Cerenkov detectors with a larger volume of water, it is estimated that for a 4 kpc supernova burst, 10^6 events will be produced in 440 kt. So this corresponds to about 20 times the Super-Kamiokande rate in the same conditions, so 100 kHz. This requirement is fulfilled by the new Super-Kamiokande data acquisition. Thus, to accept closer supernova explosion would imply an upgrade of the electronics and the filtering software.

7. Summary of the front-end requirements

The innovative concept of "smart photo-sensor" proposed by the PMm² program has led to an important study on different subjects and in particular on the front-end structure.
The front-end card has three main aims:

- Supply the 16 PMTs;
- Realize charge and time measurements (PARISROC ASIC);
- Manage the communication with the surface.

The high voltage, created in the front-end card to supply the PMTs, has required to an accurate study of the Print Circuit Board (PCB) design in terms of isolation, filtering, cooling and Electro Magnetic Compatibility (EMC).

An important analysis on the ASIC design has been done to attain the requirements deduced from the physics, the detectors structure and the PMT (explained in the previous section):

- 100% of trigger efficiency at 1/3 of p.e.
- Dynamic range up to 300 p.e.;
- Triggerless acquisition;
- 1 ns of time resolution;

- Minimum 5 kHz data rate for each PMT.

The fundamental choice to locate the front-end card underwater, close to the sensor, has induced a series of analyses on the waterproof enclosure, the card resistance to the pressure, the underwater cables and the data communication with the surface.

Chapter II

PARISROC, a Photomultiplier ARray Integrated in SiGe Read Out Chip

1. Introduction

The ASIC proposed for the PMm² project is named PARISROC acronym for *« Photomultiplier Array Integrated in SiGe Read Out Chip »*; it is a complete readout chip in AMS[30] 0.35 µm SiGe technology and it integrates 16 independent and self triggered channels to provide charge and time measurements.
The chip specifications are the following (§ 7 Chapter I):

- Variable gain to use a common high voltage for the 16 photomultipliers;
- External 50 Ω input impedance to terminate the PM cable to the ASIC;
- Auto-trigger on 1/3 of photoelectron (50 fC at PM gain of 10^6);
- Charge measurement up to 300 p.e. (50 pC);
- Time tagging better than 1 ns (TDC);
- Internal ADC.

The ASIC is designed in AMS 0.35 µm SiGe BiCMOS technology: this process of fabrication is based on the proven 0.35 µm mixed-signal CMOS process and includes an additional high performance analog oriented SiGe HBT[31] transistor module. This advanced RF-process offers high-speed HTB transistor with excellent analog performances such as high frequency and low noise [20].

This chapter will describe the ASIC architecture in all its parts and the theoretical study supported by a large number of simulation performed by the CADENCE[32] simulator.

2. ASIC description

The ASIC is a complex SoC (System on Chip) that processes the analog signals up to digitization. In this section the overall ASIC architecture is described: the analog part structure and the digital one.

[30] AustriaMicroSystems.
[31] Heterojunction Bipolar Transistor
[32] Schematic design with «Composer schematic editor» ; Simulations with «Spectre» or «Ultrasim» ; Layout «Virtuoso» ; Layout Verification «Assura».

2.1. Analog part description

The chip integrates many functions as it needs to auto-trigger asynchronously on any single photoelectron and provides digitized time and charge outputs. The 16 channels work independently and are managed by a common digital part (§ 2.2 Chapter II); the chip architecture is shown in Figure 2.1.

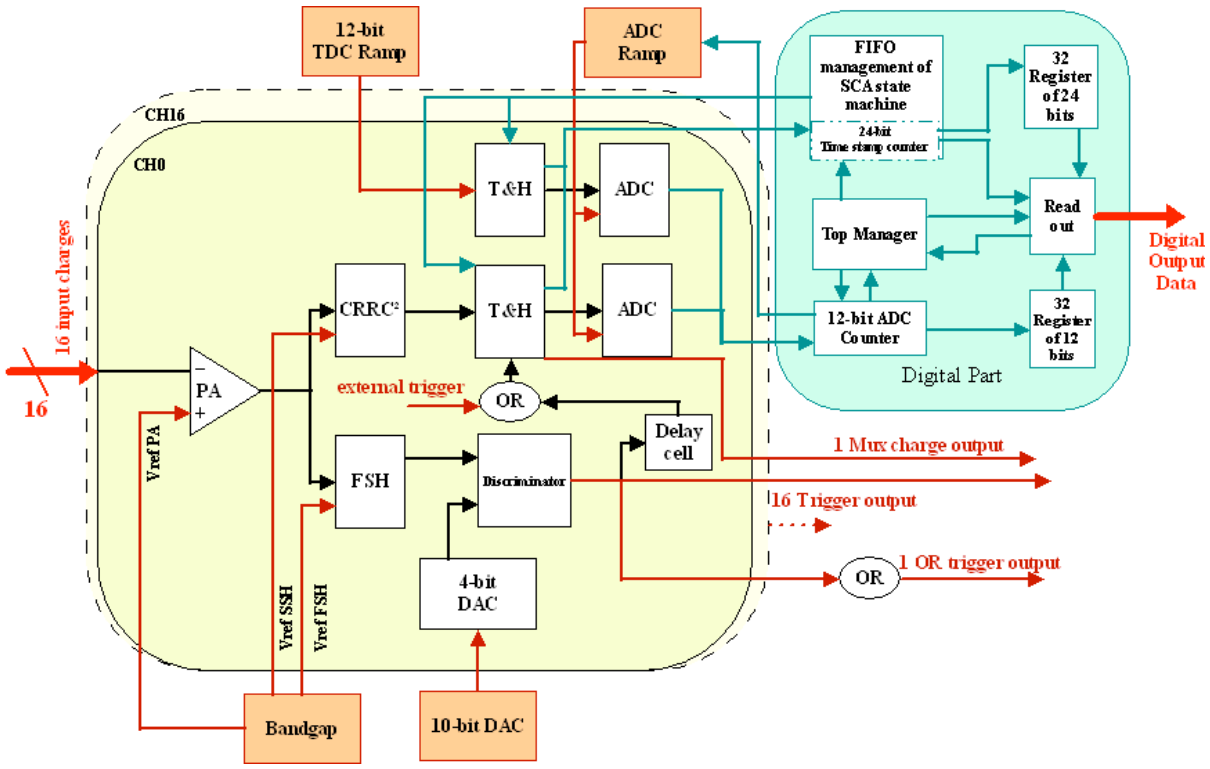

Figure 2.1. ASIC general schematic. Green block: the digital part; yellow block: analog part; orange blocks: 16 channels common blocks.

Each channel is made of an input variable gain voltage preamplifier (§ 3.2 Chapter II). The gain can be tuned simultaneously for the 16 channels by an input variable capacitance (Cin). This common gain is set by the slow control parameters which allow changing the Cin value (1pF, 2pF, 4pF) using 3 bits. The preamplifier gain is also adjustable individually channel by channel, using slow control parameters to change the variable feedback capacitance (Cf). The channel gain is set by the slow control changing Cf value (from 7 fF to 1 pF) on 8 bits.

The gain $G = \frac{Cin}{Cf}$ is, then, given by Cin and Cf.

The preamplifier is followed by a slow channel used for the charge measurements and a fast channel for the trigger production.

The slow channel (§ 4.2 Chapter II) is made of a CRRC² shaper followed by a Track and Hold (T&H) with a depth of 2 (two capacitors) to provide a linear charge measurement up to 50 pC. The T&H (§ 4.4 Chapter II), works in a "ping-pong mode": the shaper signal is sent in the first capacitor, while this charge value is digitized, a second slow shaper signal is sent in the second capacitor (Figure 2.2). This mode allows to minimize the dead time during digitization (the rate permitted is 5 kHz).

The fast channel consists of a fast shaper (15 ns) (§ 4.3 Chapter II) followed by two low offset discriminators[33] to auto-trigger down to 50 fC (1/3 p.e.). The thresholds are loaded by 2 internal 10-bit DACs common for the 16 channels and a 4-bit DAC per channel for each discriminator. The 2 discriminator outputs are multiplexed to provide only 16 trigger outputs (Figure 2.2). The trigger signal,

[33] One discriminator is enough to the ASIC; the second one is placed for additional tests.

after being delayed by a variable delay box which is tunable on 5 bits from 25 to 200 ns, is sent to the T&H cell to open the hold switch in order to save the charge as well as the time.
An "OR" of the 16 triggers gives a 17th output trigger signal.
The SCA[34] cell is made by two dual T&H cells for charge and time measurements that are then converted by two internal Wilkinson ADCs at 40 MHz (§ 4.6 Chapter II). The threshold used to convert the charge and fine time, in the ADC discriminators is provided by a common variable ramp of 8, 10 or 12 bits.
In addition an OTA follower, common to all channels, delivers an analog multiplexed charge signal output on a pin of the ASIC (Pad).
All the voltage reference values are provided by a common bandgap.
All channels are handled independently by the digital part and only the channels that have created a trigger are digitized and transferred to the internal memory and then sent-out in a data-driven way.
The detailed schematic of the analog part is shown in Figure 2.2.

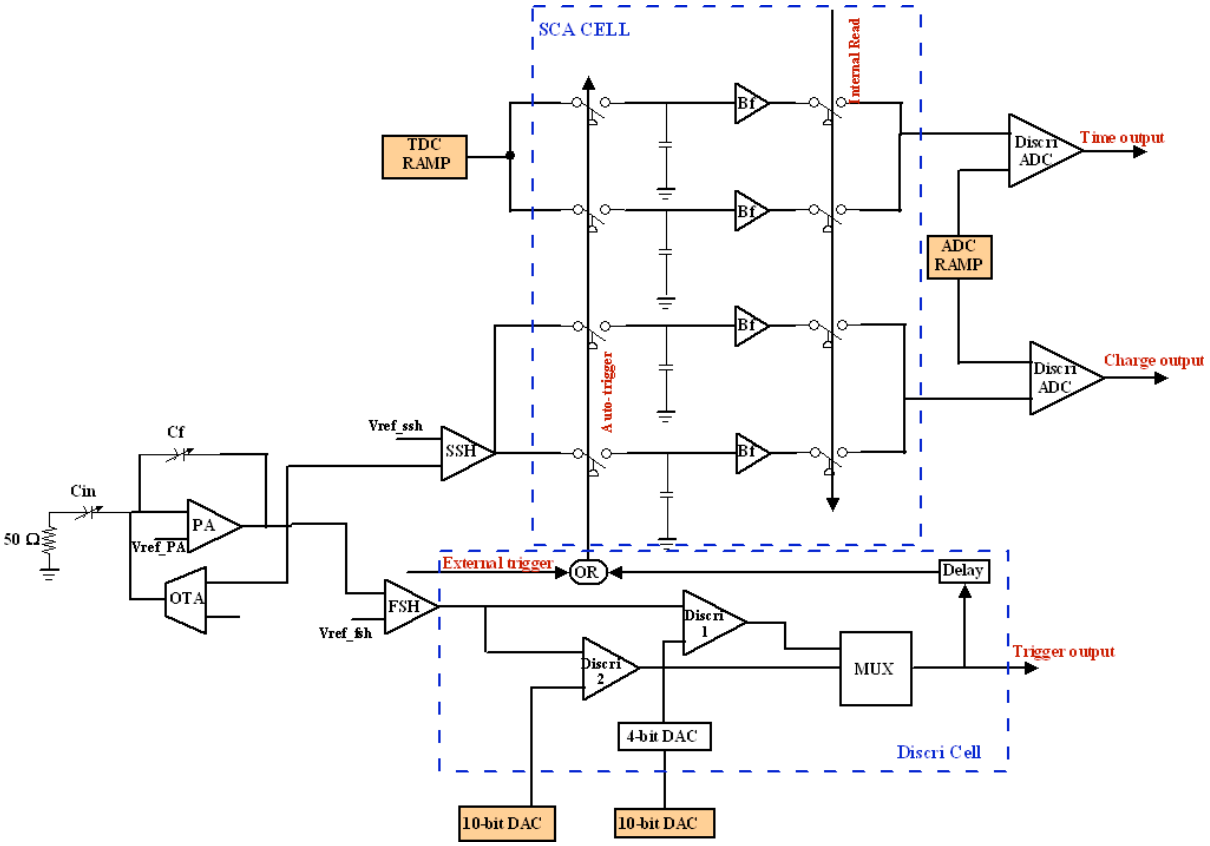

Figure 2.2. Analog part schematic.

The layout of the whole chip is exhibited in Figure 2.3:

- The digital part on the right of the picture;
- The 16 analog channels on the left;
- The TDC ramp and the ADC ramp, the bandgap and the DAC are at the bottom of the picture.

[34] Switched Capacitor Array.

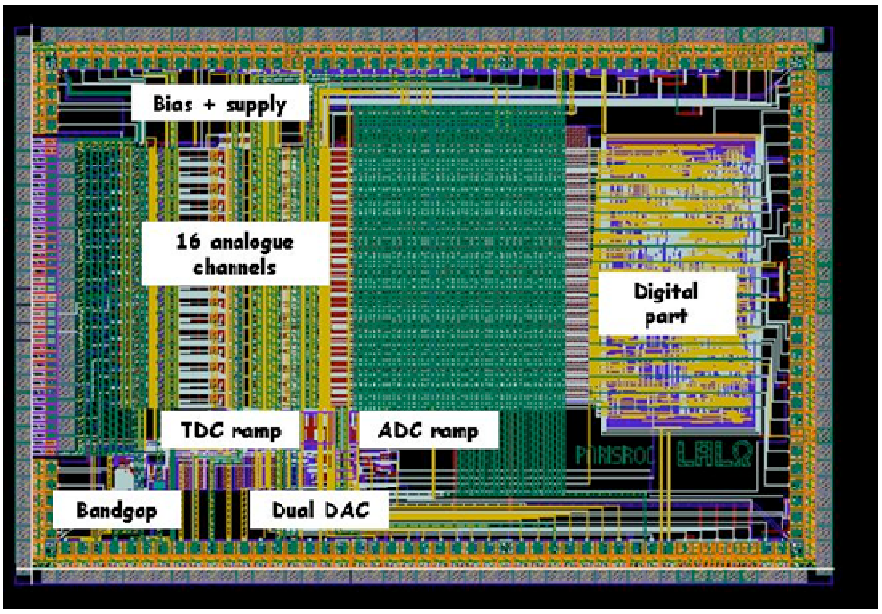

Figure 2.3. ASIC Layout; size: 5.3 mm x 3.4 mm.

2.2. Digital part

The digital part of PARISROC is built around 4 modules: acquisition, conversion, readout and top manager. PARISROC is based on 2 memories [21]. During acquisition, discriminated analog signals are stored in an SCA. The analog to digital conversion module converts analog charges and times into digital values which are saved into registers (RAM). At the end of the cycle, the RAM is readout by an external system. The block diagram is given below on Figure 2.4.

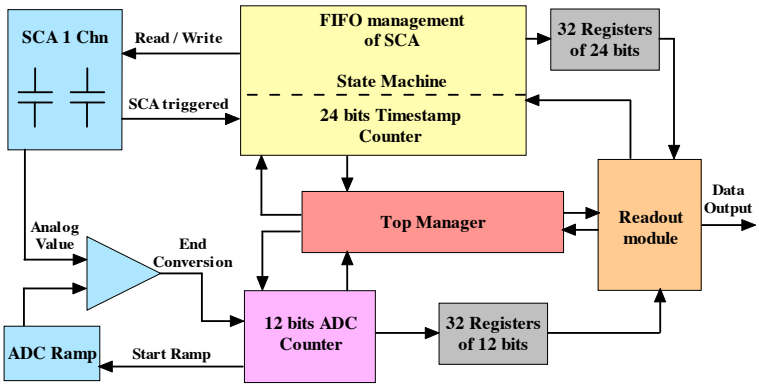

Figure 2.4. Block diagram of the digital part.

This sequence is made by the top manager module which controls the three other ones. As shown in Figure 2.5 when one or more channels are hit, it starts the ADC conversion and then the readout of the digitized data. The maximum cycle length is about 200 µs. During conversion and readout, the acquisition is still active. This means that discriminated analog signals can be stored at any time of the sequence.

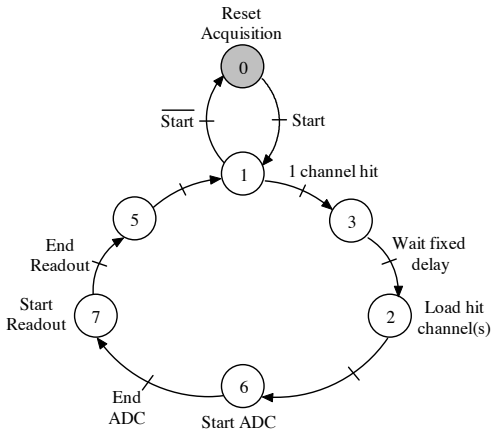

Figure 2.5. Top manager sequence.

The first module in the sequence is the acquisition which is dedicated to the charge and fine time measurements. It manages the SCA where charge and fine time are stored as a voltage as shown in Figure 2.6. It also integrates the coarse time measurement by a 24-bit gray counter with a resolution of 100 ns. Each channel has a depth of 2 for the SCA and they are managed individually in a ping-pong mode: the first signal that arrives, in one channel, is saved in the first capacitance and the second in the second one. Besides, the SCA is treated like a FIFO memory: the analog voltage can be written, read and erased from this memory.

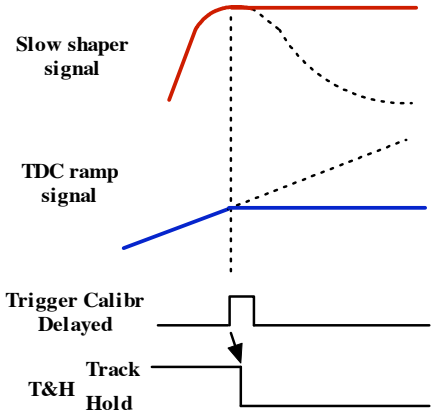

Figure 2.6. SCA analogue voltage.

The next step consists in the conversion of the stored analog values (charge and fine time: Figure 2.6) into digital ones by a Wilkinson ADC. The counter clock frequency is 40 MHz, it implies a maximum ADC conversion time of 103 µs (2^{12} x 25 ns) when it overflows. This module makes 32 conversions per run (16 charges and 16 fine times).

Finally, the readout module permits one to empty all the registers and transfer the data to an external system. As it will only transfer hit channels, this module tags each frame with its channel number. It works as a selective readout. The pattern used is composed of 4 data: 4-bit channel number, 24-bit coarse time, 12-bit charge and 12-bit fine time. The total length of one frame is 52 bits. The maximum readout time appears when all channels are hit. About 832 bits of data are transferred to the concentrator with a 10 MHz clock: the readout takes about 100 µs with 1 µs between 2 frames.

3. ASIC input stage study

The ASIC has been studied in all its parts and an important work of simulations, performed with Cadence simulator, has led to an accurate investigation of each analog block in terms of:

- Frequency behavior;
- Output waveforms;
- Noise.

The theoretical study will be mainly focused on the first stages of the analog channel and in particular on the preamplifier for its peculiar structure respect to the conventional one used in particles physics read out.

3.1. Input signal

The signal coming from the PMT is a negative fast current signal (few ns rise time) that is sent into the ASIC channel. A 50 Ω resistor is placed outside the ASIC channel input to terminate the PMT cable impedance. Therefore a voltage signal is sent to the first stage of the channel i.e. the preamplifier (Figure 2.7).

The charge injected by the PMT has a dynamic range from 0 to 50 pC which represents 0 to 300 p.e. for a PMT gain of 10^6 (1 p.e. = 160 fC). This charge dynamic range is required by the PMm² project as explained in § 6 Chapter I.
In order to reproduce this injected charge, the input signal, used in simulation, is a triangle current signal[35] with 5 ns rise and fall time and 5 ns of duration as shown in Figure 2.7. Is known that the integral of the current signal gives the charge $Q = \int_{t1}^{t2} I(t)dt$ then the input current varies from 0 to 5 mA (1 p.e ≈ 16 μA).
This current is converted in a voltage input signal through the input resistor, as explained previously, with values from 0 to 250 mV (1 p.e. ≈ 0.8 mV).

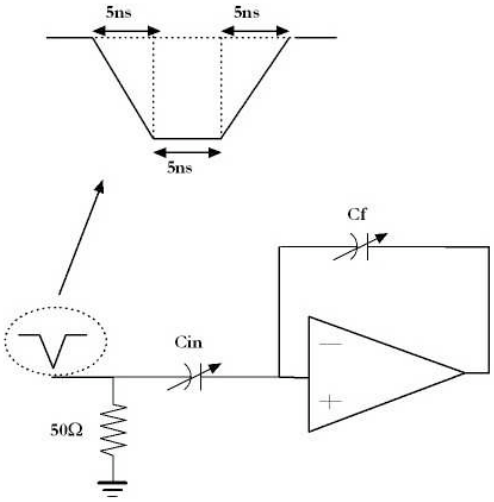

Figure 2.7. Input signal used in simulation.

[35] The pulse rise, fall and width time have been conditioned by the pulse generator used in measurements (§ 2.3 Chapter III) in order to compare these one with the simulation results.

3.2. Preamplifier

The preamplifier is needed to amplify the low level input signal by a factor around 10. Is essential to detect moderate injected charge (i.e. 1 p.e.) and is one of the most critical parts of the design considering that it is the first stage of the chain. This brought to some constraints as:

- A fast response. It must handle usually fast input pulses;
- A good linearity for a wide input dynamic range;
- A low noise structure, in order to avoid the amplification of the noise that will be injected in the further stages.

The preamplifier, designed for PARISROC ASIC, is a voltage preamplifier (Figure 2.8) conceived to read an input voltage signal and to have a variable and adjustable gain in order to modify, respectively, the gain in all channels relative to the PMT and the gain in each channel to compensate for possible non uniformity of the 16 PMT gains in the array (factor 4)[36] [16].

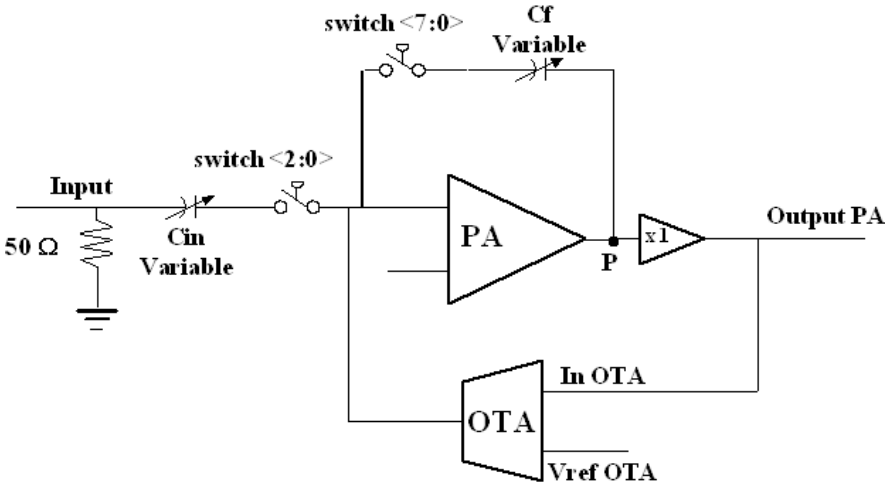

Figure 2.8. General preamplifier structure.

3.2.1. General description of the preamplifier

The preamplifier uses a typical cascode structure: a transconductance amplifier followed by a current buffer and an output voltage follower (Figure 2.9).
This structure gives the well known advantages: it improves the input-output isolation, increases the input and output impedances as well as the gain or the bandwidth. Indeed by improving the input-output isolation, the Miller effect is eliminated. This contributes also to a higher bandwidth.
The input transistor (P1) (Figure 2.9) is a PMOS transistor in common source configuration; the choice of an input PMOS is due to the 1/f noise minimization (§ 3.5.1 Chapter II) and to the ultra low leakage current. The transistor P1 has W = 800 μm; L = 0.35 μm; its significant size induces a large gm and then a lower series noise. The size of the cascode transistor (P2) is W = 100 μm; L = 0.35 μm must be chosen to reach high speed preamplifier performance.

[36] The engineers of the Photonic Company have demonstrated that for a large PMTs production and selecting the good ones the gain dispersion of 4 can be reached.

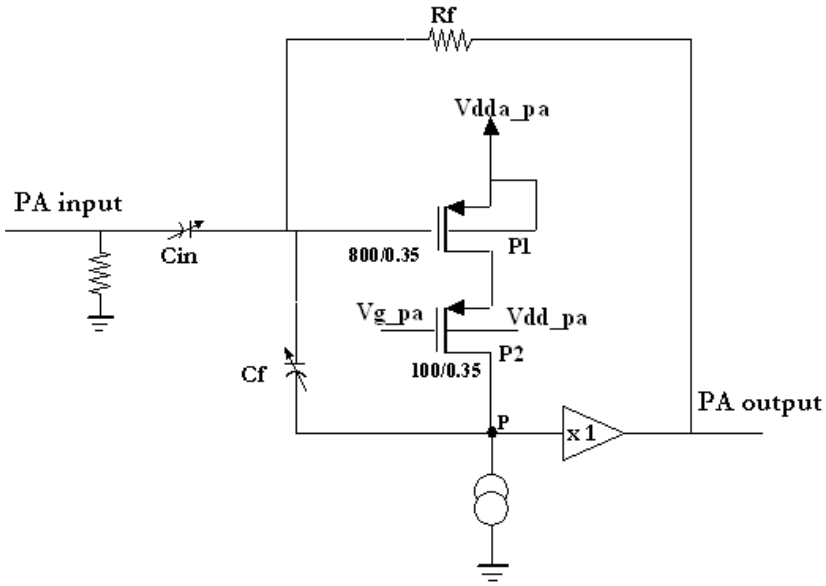

Figure 2.9. Internal preamplifier structure.

An output buffer is designed in order to provide low impedance for voltage drivers output. The input dc level is high (about 2.6 V) whereas the output dc level is low (about 1 V).
The preamplifier feedback (see Figure 2.9) has a peculiar structure; the traditional resistor is replaced by:

- An OTA, that will be described in § 3.3 Chapter II, connected from the input to the output of the preamplifier (for DC feedback);
- The capacitor Cf that has two functionalities the charge integration and the preamplifier frequency compensation. This feedback capacitance Cf is connected between the preamplifier input and the preamplifier output before the buffer since, as explained in the next section, the dominant pole is located at this point.

3.2.2. Preamplifier theoretical study

In this section, a detailed theoretical study of the frequency response, impedance and noise of the preamplifier is exposed. It is often compared to simulation results.
The characteristics of the transistors used (see Figure 2.10 which gives a detailed schematic of the preamplifier) are listed in the Table 2.1 and Table 2.2.

	W µm /L µm	VG (V)	VS (V)	VD (V)	Vgs (V)	Id (A)	gm (A/V)	gds (µA/V)
Q1	800/0.35	2.7	3.5	916 m	-833 m	-887 µ	11.13 m	390
Q2	100/0.35	1.8	3	916 m	-1.1	-887 µ	4.2 m	162
Q3 and Q4	20/1	1.4	916 m	200 m	1.1	444 µ	1.3 m	24
Q5	50/0.35	916 m	1.8	0	-858 m	-111 µ	1.1 m	34
Q6	20/1	2.3	3.5	1.8	-1.2	-113 µ	417 µ	4.3
Q7	20/1	1.2	0	972 m	1.2	553 µ	1.4 m	17

Table 2.1. Preamplifier MOS parameters.

	Vb (V)	Ve (mV)	Vc (V)	Vbe (mV)	Ic (µA)	β	gm (mA/V)
Q8	1.8	972	3.5	802	551	272	20

Table 2.2. Preamplifier BJT characteristics.

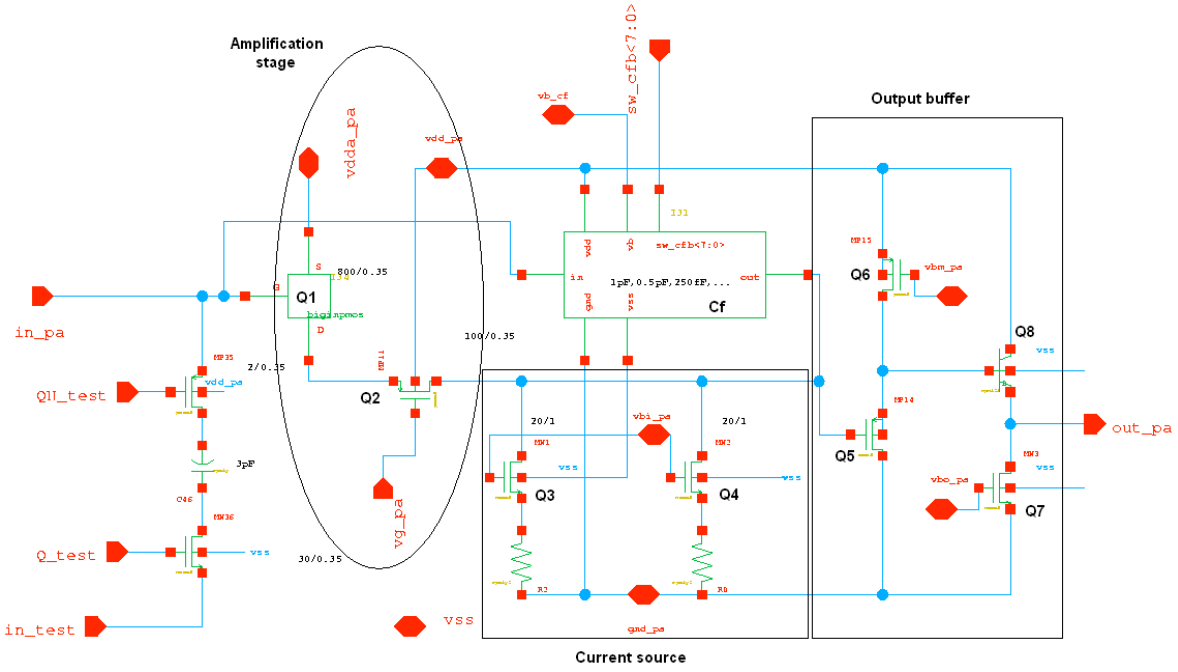

Figure 2.10. Preamplifier detailed schematic.

3.2.3. Open loop gain

The impedance *Rp* seen on the output node P (on Figure 2.9) is given by:

$$R_p = Ro^* // r^* \qquad (2.\ 1)$$

With:

- $Ro^* \cong gm_2 ro_1 ro_2 = 66.5k\Omega$ with $ro_1 = \frac{1}{gds_1}$ (Q1 transistor) and $ro_2 = \frac{1}{gds_2}$ (Q2 transistor);
- r* is due to the two transistors, Q3 and Q4, that make the current source: $r^* = ro_3 // ro_4$

As the current source is degenerated by R_{deg}, its output resistance is given by:

$$ro = \frac{1}{gds}(1 + gmR_{deg}) \qquad (2.\ 2)$$

Resulting in a total value of:

$$r^* = \frac{1}{2gds}(1 + gmR_{deg}) = 34.4k\Omega \qquad (2.\ 3)$$

with *gds= gds3= gds4= 24 µA/V*, *gm= gm3= gm4= 1.3 mA/V* and R_{deg} (degeneration resistor)= 500 Ω. The impedance *Rp* has a theoretical value of *22.7 kΩ* which is in good agreement with simulation result of 25 kΩ [37] shown below in Figure 2.11. All the following simulations are performed with Cin 4 pF and Cf 0.5 pF.

[37] In simulation, a current of 1 A is injected in the preamplifier output with the preamplifier input put to the ground. The output voltage trend versus the frequency gives the preamplifier output impedance.

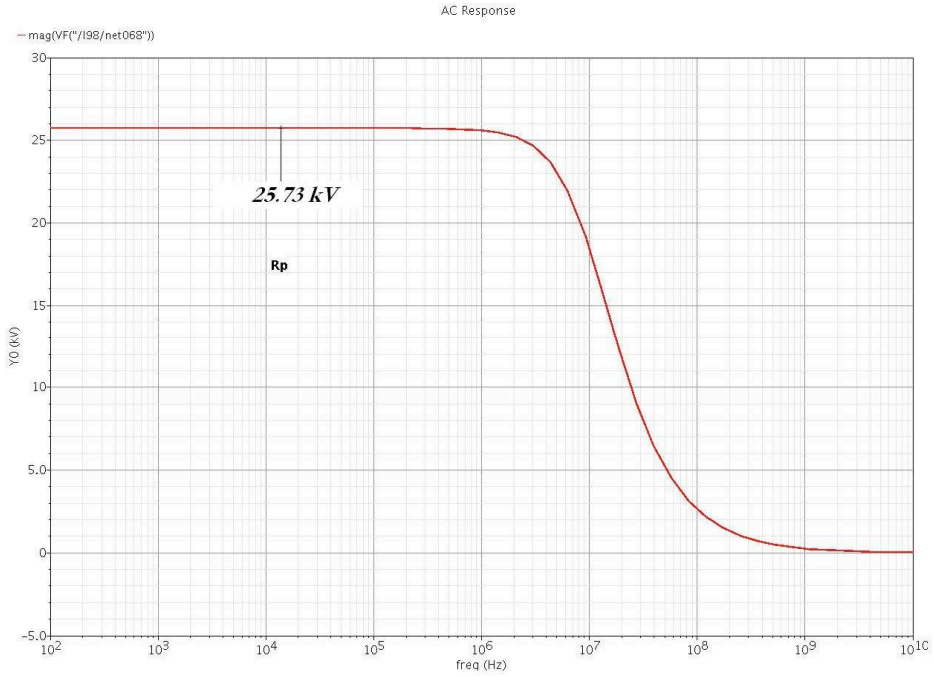

Figure 2.11. Simulated preamplifier output resistance.

The preamplifier's *Open Loop Gain* $G(\omega)$ can be written as follows:

$$G(\omega) = \frac{gm_1 \times R_p}{(1 + s\tau_0)(1 + s\tau_2)} \qquad (2.4)$$

Where R_p is the impedance seen at the node P (calculated above), $gm_1 = 11\ mA/V$, $\tau_0 = RpCp$ that gives first pole p_0 at $\omega_0 = \frac{1}{R_p C_p}$ and τ_2 gives the second pole p_2 usually considered negligible.

Thus the low frequency open loop theoretical value ($gm_1 \times R_p$) is 253 which is in good agreement with the simulation (Figure 2.12).

Cp is equal to Cf plus the parasitic capacitance of the transistor which has been extracted and found equal to 170 fF. Therefore the frequency of the first pole is 10 MHz as obtained in the simulation and is displayed in the following figure. The characteristics of the preamplifier are summarized below:

- Open Loop gain[38] = 48.5 dB = 265;
- f (-3dB) = 10 MHz;
- Cut off frequency = ft = 1.6 GHz.

[38] The simulation open loop gain is obtained injecting a current signal (ac) in the input and opening the feedback. The preamplifier output voltage trend (in dB) is plotted versus the frequency.

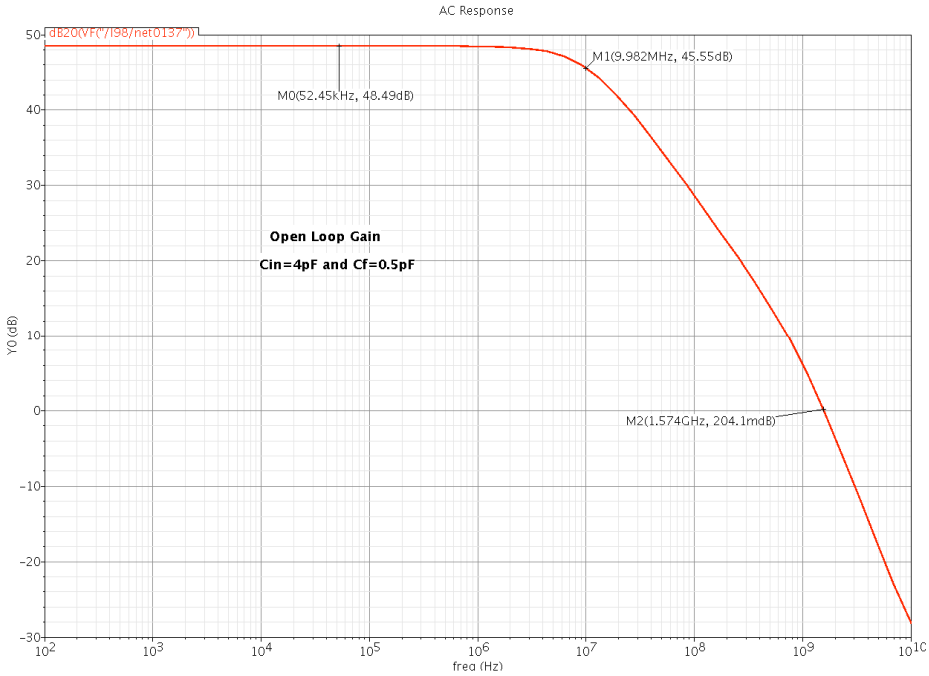

Figure 2.12. Simulated preamplifier open loop gain. With Cin = 4 pF and Cf = 0.5 pF.

A. Closed loop gain

a. Frequency response

The closed loop gain is given by the following expression:

$$\frac{V_{out}(\omega)}{V_{in}(\omega)} = -\frac{Z_f}{Z_{in}}\frac{\beta(\omega)G(\omega)}{1+\beta(\omega)G(\omega)} = -\frac{Z_f}{Z_{in}}\frac{1}{1+\frac{1}{\beta(\omega)G(\omega)}} \qquad (2.\ 5)$$

with $\beta(\omega) = \frac{Z_t}{(Z_f + Z_t)}$ *and* $\frac{1}{Z_t} = \frac{1}{Z_p} + \frac{1}{Z_{in}}$; Z_p the input parasitic impedance (Figure 2.13).

With $Zf = \frac{1}{\omega Cf}$ and $Cf = 0.5\,pF$; $Zi = \frac{1}{\omega Cin}$ and $Cin = 4\,pF$; supposing $Z_p << Z_{in}$ then $\frac{1}{\beta} = \frac{Cin + Cf}{Cf} = 9$ i.e. 19 dB.

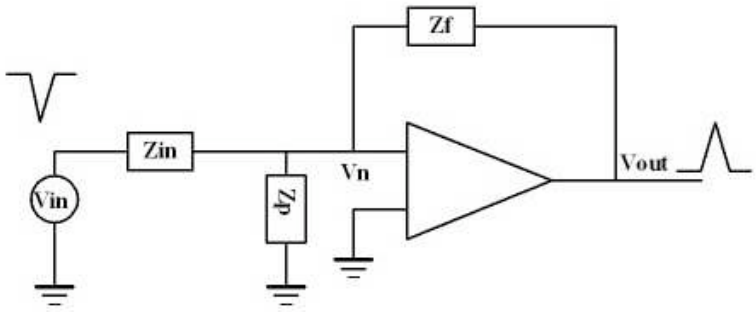

Figure 2.13. Preamplifier general schematic for frequency study.

So to ensure the stability $\beta(\omega)G(\omega)$ must be different from -1 i.e. $|\beta(\omega)G(\omega)| \neq 1$ and the phase $\varphi \neq -180°$.

For $G(\omega) = 19dB$, $f = 310MHz$ and the phase is equal to 95° (Figure 2.14).

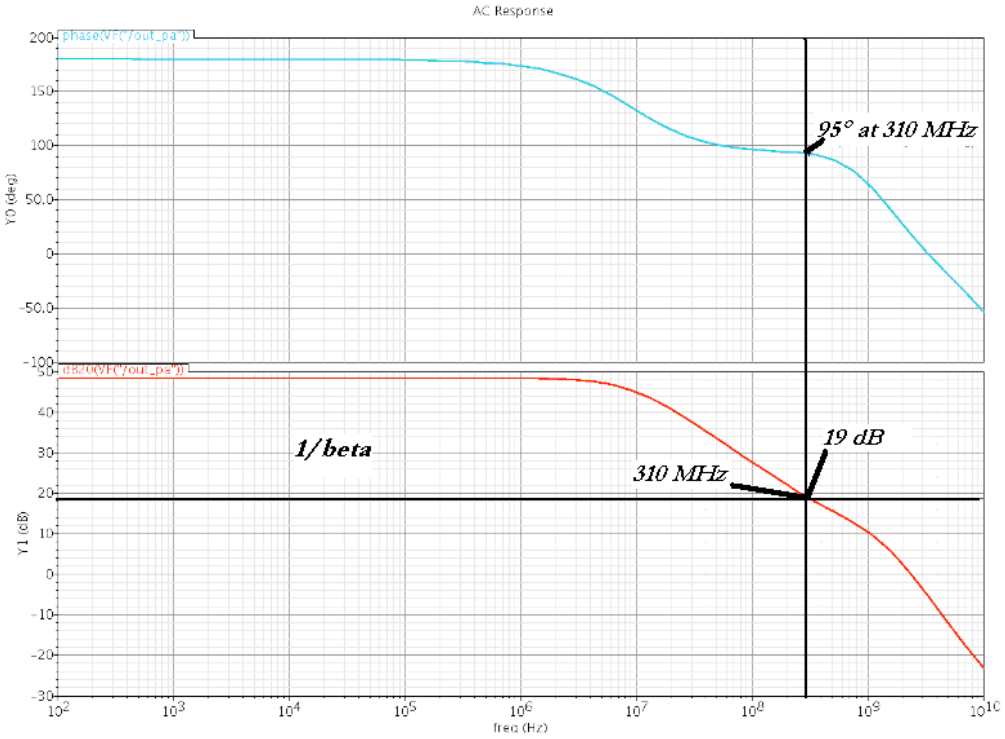

Figure 2.14. Simulated preamplifier phase margin.

b. Time response

In the following calculations, we suppose that the preamplifier has only one pole ω_0. The 2nd pole is indeed located at about 1 GHz and can be neglected. Thus the open loop gain of the preamplifier can be written as follows:

$$G(\omega) = \frac{G_O}{1 + j\frac{\omega}{\omega_0}} \qquad (2.\ 6)$$

with $G_0 = g_m R_p$ and $\omega_0 = \frac{1}{R_p C_p}$.

From equation (2.5) with $\frac{1}{\beta} = \frac{Cin + Cf}{Cf}$ and equation (2.6):

$$\frac{Vout(\omega)}{Vin(\omega)} \approx -\frac{Cin}{Cf}\left(\frac{1}{1 + \frac{Cin + Cf}{CfG(\omega)}}\right) = -\frac{Cin}{Cf}\left(\frac{1}{1 + \frac{Cin + Cf}{CfG_0} + \frac{Cin + Cf}{G_0\omega_0 Cf} j\omega}\right) = \qquad (2.\ 7)$$

$$= -\frac{Cin}{Cf}\left(\frac{1}{1 + \omega_0\omega_{pa} + j\frac{\omega}{\omega_{pa}}}\right)$$

With $\omega_{pa} = \frac{G_0\omega_0 Cf}{Cin + Cf}$.

It is assumed that $\frac{Cin+Cf}{CfG_0} << 1$ therefore we get:

$$\frac{Vout(\omega)}{Vin(\omega)} = -\frac{Cin}{Cf}\left(\frac{1}{1+j\frac{\omega}{\omega_{pa}}}\right) \qquad (2.\ 8)$$

With Dirac voltage signal at the preamplifier input equivalent to a charge Qo(s) and $\tau_i = \frac{Cin+Cf}{CfG_0\omega_0}$

$$Vout(s) \approx -\frac{Cin}{Cf}\left(\frac{Qo}{1+\tau_i s}\right) \qquad (2.\ 9)$$

$$Vout(t) = L^{-1}\left[-\frac{Cin}{Cf}\left(\frac{Qo}{1+\tau_i s}\right)\right] = -\frac{CinQo}{Cf}e^{\frac{-t}{\tau_i}} \qquad (2.\ 10)$$

3.2.4. Preamplifier output signal and linearity

The main characteristic of the preamplifier is its variable gain[39] obtained by the switched input (Cin) and feedback (Cf) capacitors.
In Figure 2.15 are shown the preamplifier output waveforms for a fixed gain and different input signal (top plot) and for a fixed input signal and a different preamplifier gain (bottom plot). The shape of the output signals (i.e. their rise time) depends from the input Cin switched structure as will be explained in § 3.4 Chapter II.

[39] Preamplifier gain is $\frac{Cin}{Cf}$.

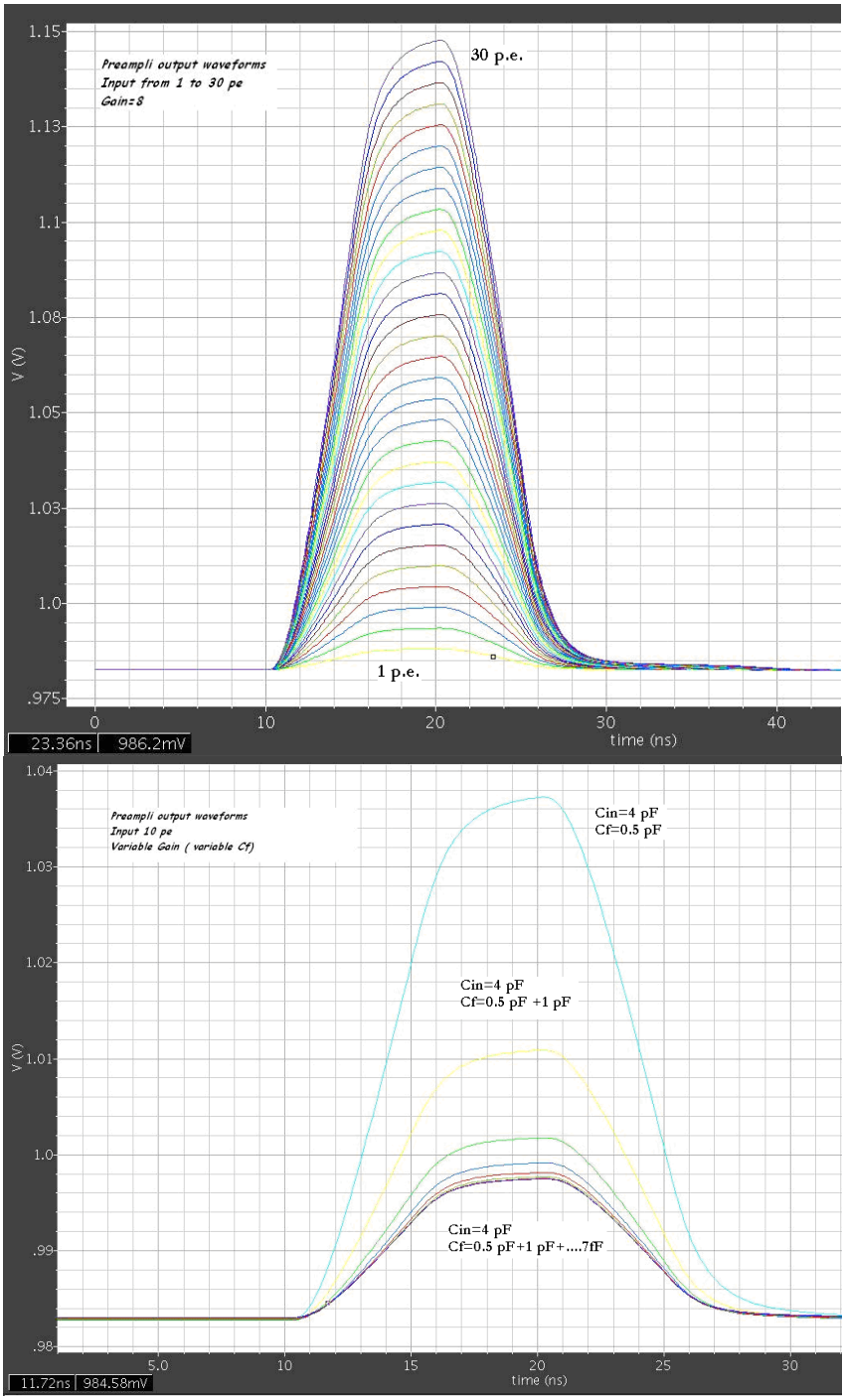

Figure 2.15. Simulated preamplifier output waveforms for different input signals with fixed gain 8(top plot) and for fixed input signal 10 p.e. at different gains (different feedback capacitor values bottom plot).

Figure 2.16 represents the preamplifier output waveform for an input signal of 1 p.e. which is equivalent to an input signal of ~800 μV. The maximum voltage signal obtained is 5.5 mV resulting in a gain of 7 (theoretical gain of 8) with a rise time of 5 ns.

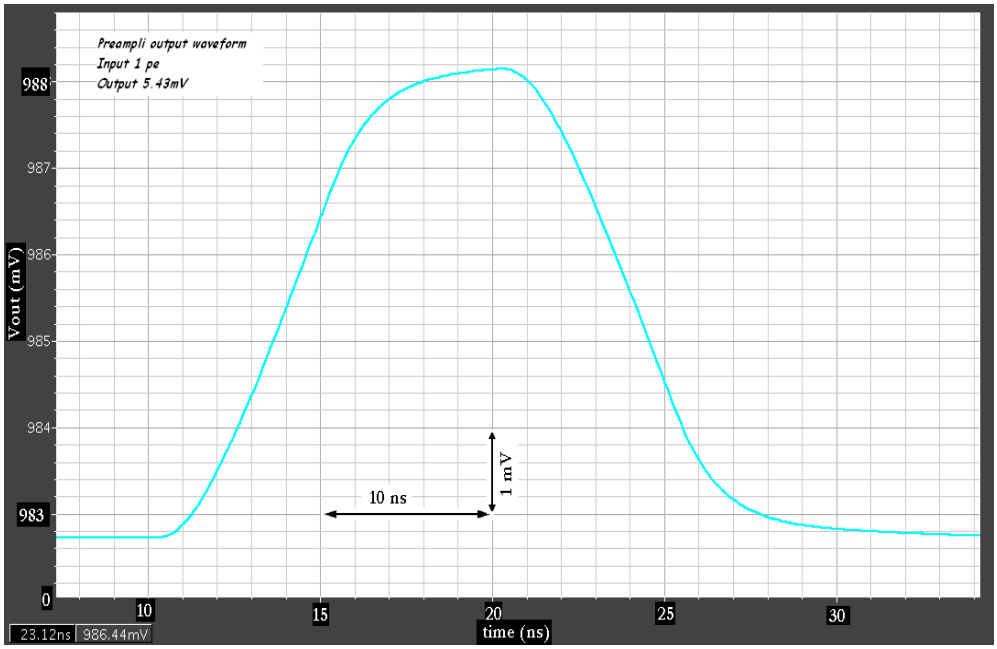

Figure 2.16. Simulated preamplifier 1 p.e. output waveform.

The preamplifier linearity as a function of the input dynamic range is displayed in Figure 2.17.
The maximum preamplifier output value is simulated and plotted as a function of the injected charge (from 0 to 300 pe[40]) for different preamplifier gains: respectively red, blue and green curves for gain of 8, 4 and 2.
Table 2.3 lists the residuals obtained for the different gains showing a good linearity (better than ± 1%). The linearity for a preamplifier gain of 8 yelds a dynamic range of 250 p.e., which is a very good result considering that big values of preamplifier gains are associated to small input charges.

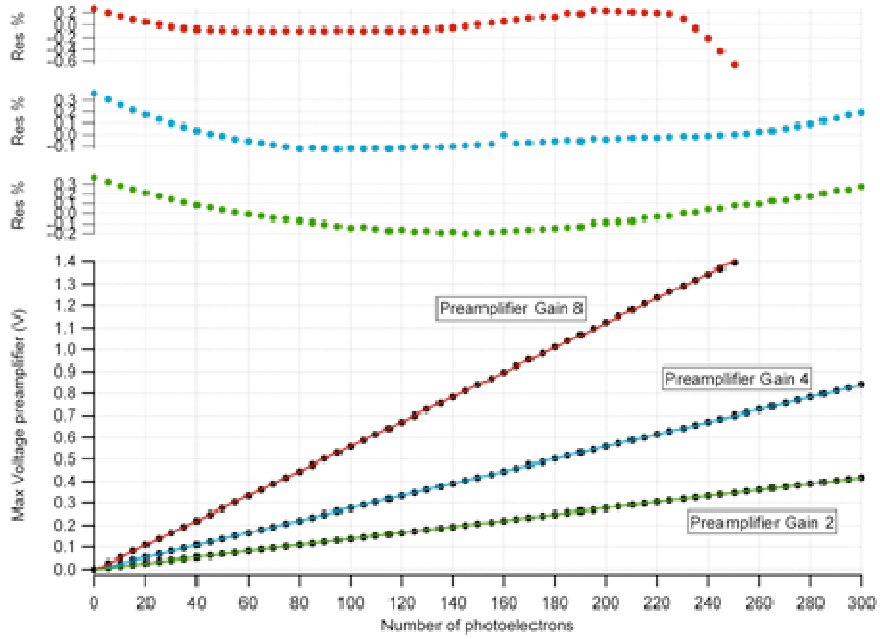

Figure 2.17. Simulated preamplifier linearity. Red curve: residuals and fit for preamplifier gain 8; Blue curve: residuals and fit for preamplifier gain 4; Green curve: residuals and fit for preamplifier gain 2.

[40] The input dynamic range for linearity simulation corresponds to the one required to the project; for small preamplifier gains the trend can be linear up to considerable values.

Preamplifier Gain	Preamplifier output maximum amplitude (V)	Maximum Charge, Corresponding number of p.e.	Residuals (%)
8	1.4	40 pC, 250 p.e.	-0.6 to 0.2 %
4	0.8	48 pC, 300 p.e.	-0.1 to 0.3 %
2	0.4	48 pC, 300 p.e.	-0.2 to 0.3 %

Table 2.3. Preamplifier linearity for gains 8, 4 and 2.

3.3. OTA structure

As explained in § 3.2.1 Chapter II an OTA replaces the traditional feedback resistor (Rf). This atypical feedback will be studied in this section.
A classical feedback resistor Rf exhibits a parallel noise equal to:

$$Si(\omega) = \frac{4kT}{Rf} \qquad (2.\ 11)$$

This noise is, usually, a dominant term in the preamplifier feedback noise calculation thus a large feedback resistor is used to reduce the noise.
The important equivalent impedance of an OTA is indeed very convenient to avoid a large Rf which is difficult to integrate.

According to the preamplifier dc level, p-type input stage and n-type second differential stage are used so that both the OTA input and output dynamic ranges are not limited (Figure 2.18). The input p-type stage is a simple follower which acts as a voltage shifter. The second stage acts as a differential-to-single transformer and in fact provides the output dc for this amplifier.

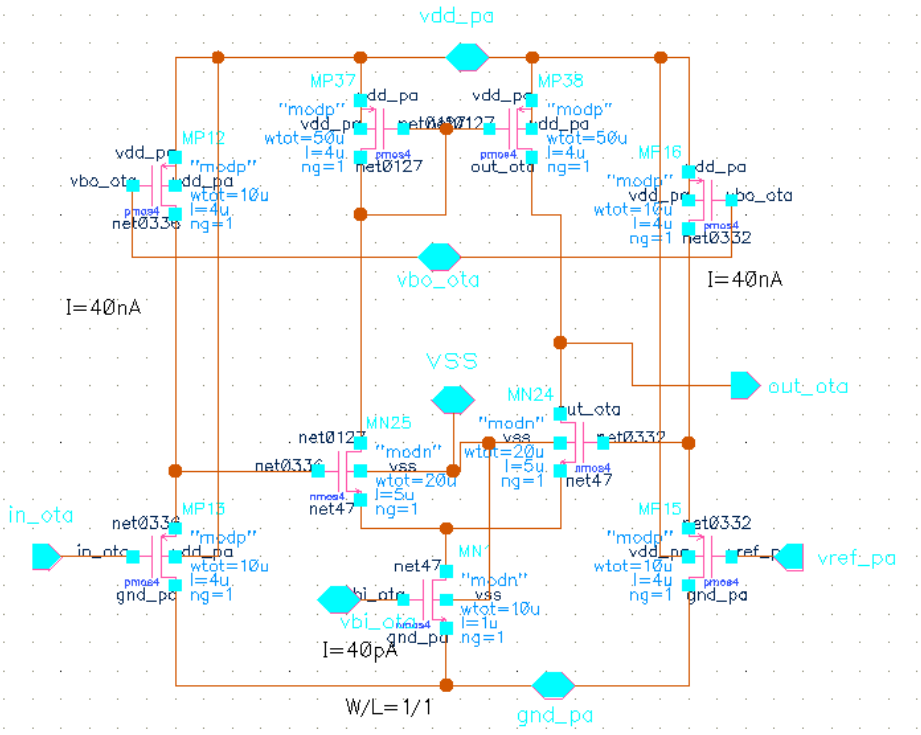

Figure 2.18. Ota detailed schematics.

In this structure, the output of the differential stage is in fact connected to the input of the preamplifier therefore the current of the differential stage was designed to be as low as pA in order to minimize the equivalent leakage current of the preamplifier and thus minimize the parallel noise.
The input stage of the OTA is connected to the output of the preamplifier.
To stabilize the dc level of the preamplifier:

- The OTA bandwidth has been minimized in order to make it insensitive to the preamplifier fast signals;
- The current of the OTA first stage has been set relatively small (nA) so that the first stage not only works as a voltage shifter, but also clips large input signals.

Figure 2.19 gives a simplified version of the OTA schematic (Figure 2.18) where Q1 and Q2 are the transistors of the differential pair and Q3 and Q4 the transistors of the active load; Cm the capacitor on the drain of the input transistor of the differential pair; Cout the output capacitor on the drain of the output transistor of the differential pair. The OTA parameters, used for the theoretical study, are listed in Table 2.4.

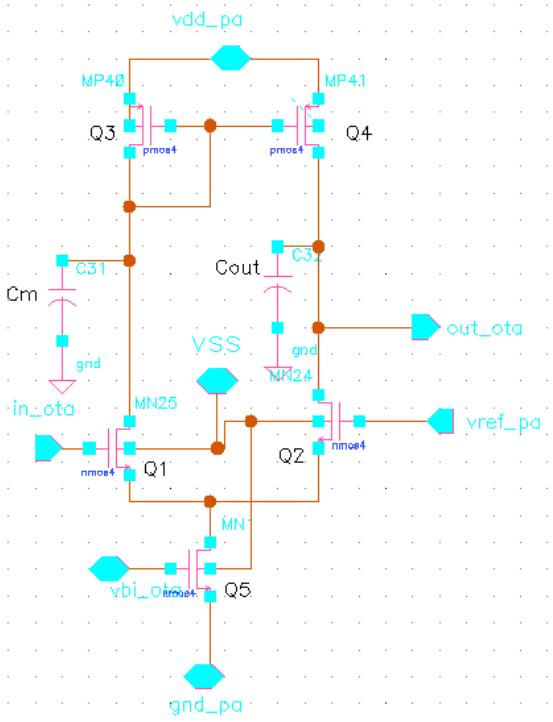

Figure 2.19. Simplified OTA schematic for theoretical study.

	W µm /L µm	VG (V)	VS (V)	VD (V)	Vgs (V)	Id (A)	gm (A/V)	gds (A/V)
Q1	20/5	1.9	1.3	2.9	563 m	355 p	11.3 n	7 p
Q2	20/5	1.9	1.3	2.9	563 m	355 p	11.3 n	7 p
Q3	50/4	2.9	3.3	2.9	408 m	356 p	10.7 n	5 p
Q4	50/4	2.9	3.3	2.9	408 m	356 p	10.7 n	5 p

Table 2.4. OTA parameters.

Using the parameters on table 2.4, the differential stage analysis is given below:

$$Vout = gm_1 vi \times \left(\frac{1 + \frac{sC_m}{2gm_3}}{1 + \frac{sC_m}{gm_3}} \right) \times \left(\frac{R_{out}}{1 + sR_{out}C_{out}} \right) \qquad (2.\ 12)$$

With $gm_1 = gm_2 = gm = 11.3\ nA/V$; $gm_3 = 10.7\ nA/V$; $g_{DS2} = 7\ pA/V$ and $g_{DS4} = 5\ pA/V$ the results are:

- First pole is given by $\tau_1 = R_{out}C_{out}$, with C_{out} ~ f F and Rout ~10^9 Ω (Equation 2.14), it is at the level of the Hz;
- The second pole is given by $\tau_2 = \frac{C_m}{gm_3}$, with C_m ~ f F, it is around the 10^6 Hz.

The low frequency voltage gain is given by:

$$A_v = gmR_{out} \qquad (2.\ 13)$$

$$R_{out} = \frac{1}{g_{DS2} + g_{DS4}} = 82 \times 10^9\ \Omega \qquad (2.\ 14)$$

$$A_v = 930 = 59dB \qquad (2.\ 15)$$

The simulation results give (Figure 2.20) a low frequency voltage gain of 56 dB and f_{-3dB} = 29 Hz.
As: $f_{-3dB} = \frac{1}{2\pi R_{out}C_{out}}$ we get 67 fF as the value of the total output capacitor C_{out}.

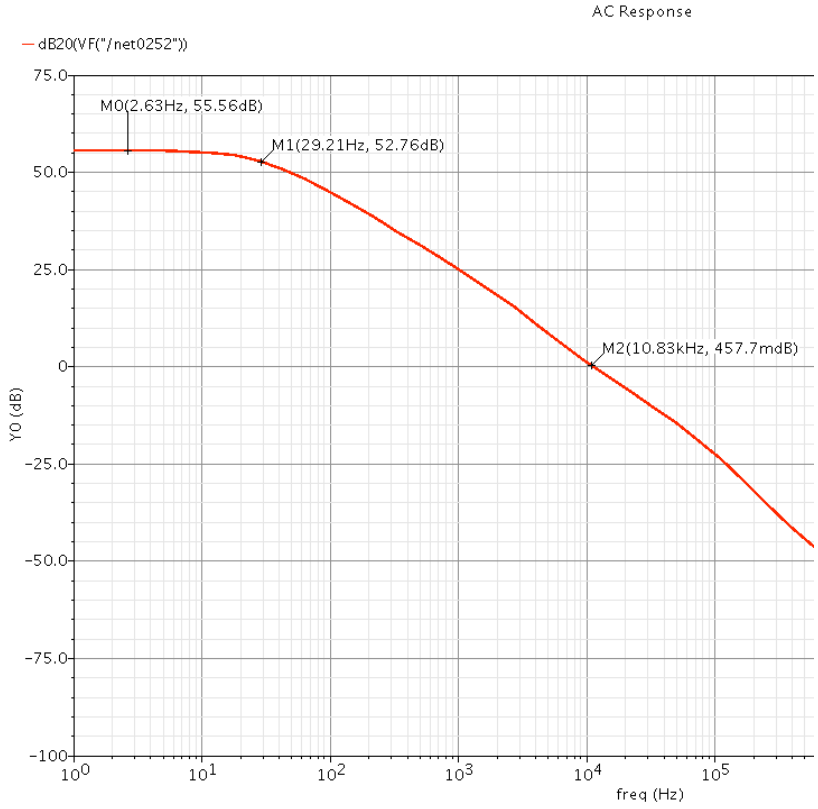

Figure 2.20. Simulated OTA open loop gain.

To study the OTA in transimpedance configuration is added in simulation a R_L= 1Ω in series with a huge capacitor C_L= 100 kF to preserve the OTA DC bias point (Figure 2. 21).

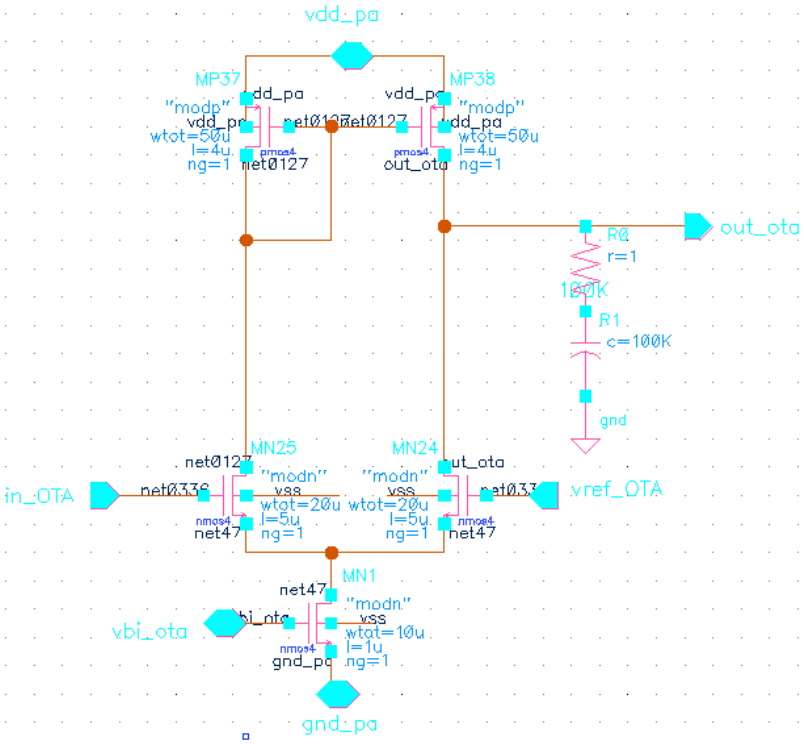

Figure 2. 21. OTA simulation schematic to calculate the equivalent impedance.

Therefore $\frac{iout}{vin} = Gm$ thus $Rf_{eq} \cong \frac{1}{Gm}$ but the poles in Gm affect the frequency response as: $Gm(f) = \frac{Gm_o}{1 + \frac{f}{f_o}}$ that gives $Zf_{eq} = \frac{1}{Gm} \cong \frac{1}{Gm_o} + j\frac{f}{f_0 Gm_0}$

Then the equivalent feedback impendence is given by a resistance $Rf = \frac{1}{Gm_0}$ and an inductance $Lf = \frac{1}{f_0 Gm_0}$.

The simulation gives for Gm the plot on Figure 2.22, yielding Gm_0= -159 dB and f_0= 4.5 kHz.

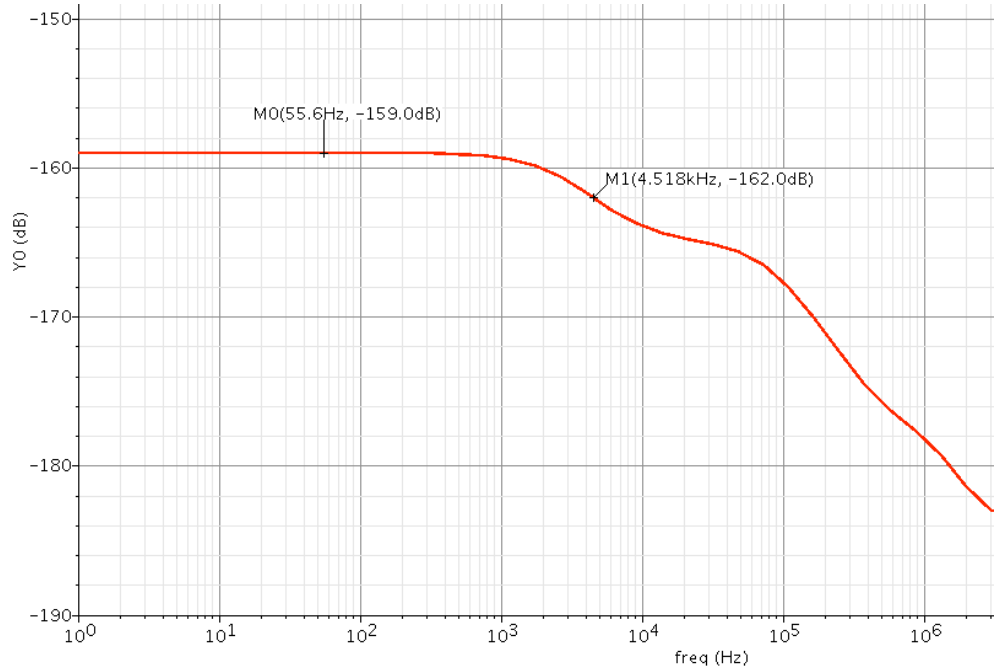

Figure 2.22. Simulated OTA Gm.

$$Gm_0(dB) = -159dB \Rightarrow Gm_0 = 10^{-8} \qquad (2.\ 16)$$

In the low frequency domain the impedance is therefore equivalent to a resistor of:

$$Rf_{eq} = 10^8\,\Omega \qquad (2.\ 17)$$

3.4. Variable capacitors structures

As said in section 2.1 the two capacitors Cin and Cf have different purposes: Cin is used to adjust the common gain value for the 16 channels (over 3 bits: 1 pF, 2 pF, 4 pF); while Cf allows setting a gain value different for each channel (on 8 bits: from 8 fF to 2 pF with steps of 8 fF).
In the phase of the preamplifier linearity study some singular behaviors have been observed and related to the Cin and Cf uncommon structures. Therefore their peculiar location in the input and feedback of the first stage has necessitated an accurate study that will be presented in this section.

As illustrated in the following pictures (Figure 2.23 and Figure 2.24), Cin is variable thanks to a switched system of three switched parallel capacitors and Cf is made using the same structure with eight switched capacitors.

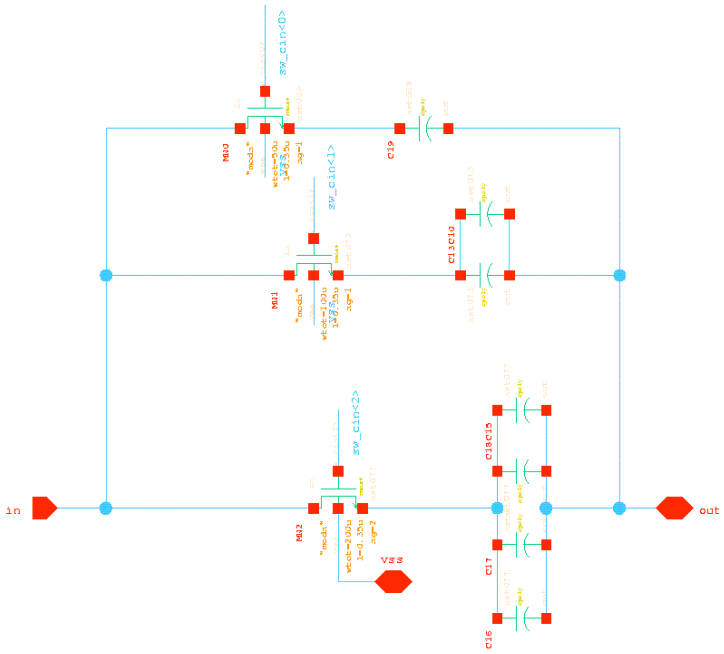

Figure 2.23. Cin first schematic.

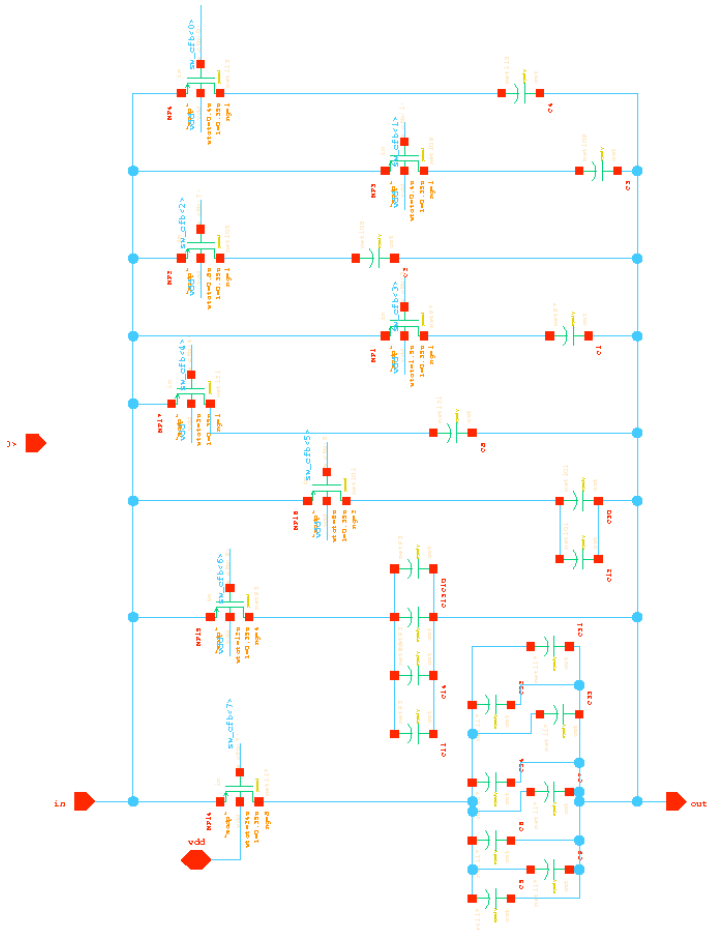

Figure 2.24. Cf first schematics.

In this phase, the input signal, used for the simulations, described in this section, is a squared signal with a pulse width of 10 ns, a rise and a fall time of 100 ps (Figure 2.25). With these characteristics the 1/3 to 300 pe input dynamic range corresponds to an input current signal varying from 5 µA to 5 mA.

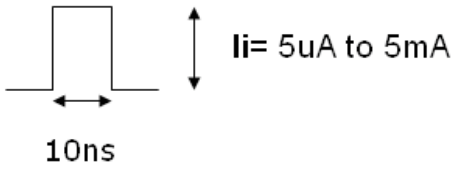

Figure 2.25. Input signal used in variable capacitance simulations.

A. Cin structure

The choice of a NMOS Cin switched structure (Figure 2.26) and the switches position before the capacitors take into account the input DC value of the preamplifier.
The NMOS switch dimensions for each capacitance values are:

- For Cin= 4 pF $\left(\frac{W}{L}\right)_1 = \frac{201\mu m}{0.35\mu m}$;
- For Cin= 2 pF $\left(\frac{W}{L}\right)_2 = \frac{102\mu m}{0.35\mu m}$;
- For Cin= 1 pF $\left(\frac{W}{L}\right)_2 = \frac{51\mu m}{0.35\mu m}$

The switches are chosen large enough to minimize their series noise when is closed and small enough to reduce parasitic capacitances.
A first study of the preamplifier behavior shows that, for a small value of preamplifier gain[41] and an important input signal, the preamplifier linearity and the output waveforms have limited performances.
In the Figure 2.26 are represented the preamplifier linearity curves and the output waveforms for a preamplifier gain 2 and for an input dynamic range from 0 to 500 p.e. Although this large input dynamic range is not required it is however important that the preamplifier exhibits good linearity performance for small gains and such dynamic ranges.

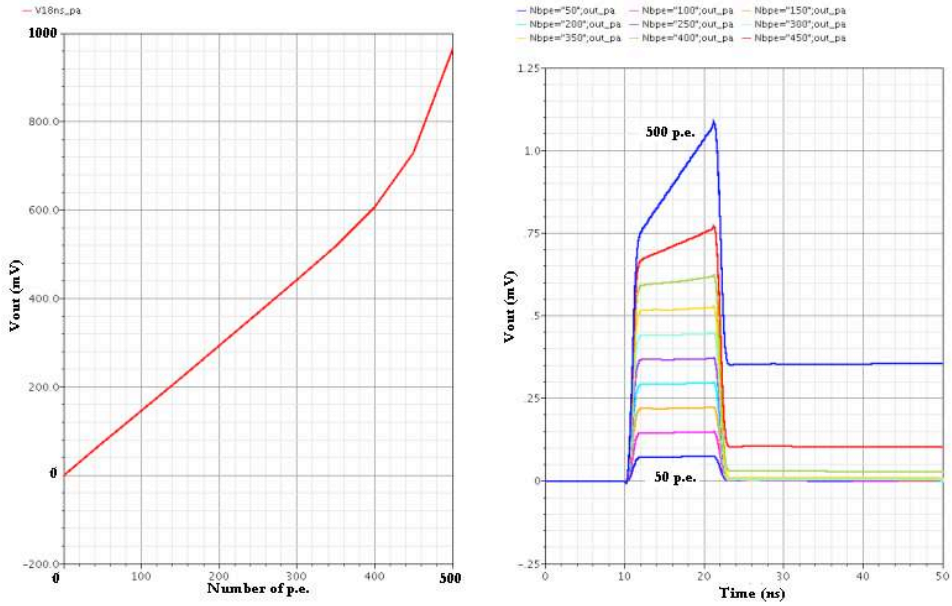

Figure 2.26. Preamplifier linearity for gain 2 (Cin= 1 pF and Cf= 0.5 pF) with first Cin schematic Left panel the maximum preamplifier value is plotted versus the injected signal until 500 p.e.; Right panel the corresponding preamplifier output signals are shown corresponding to injected charge steps of 50 p.e..

[41] For example G=2 with *Cin*=1pF and *Cf*=0.5pF.

To understand if this behavior is due to the input or the feedback capacitor, the preamplifier linearity is simulated respectively with ideal Cin and Cf or using the switches. The results are represented on Figure 2.27. A clear difference can be observed with better linearity obtained when Cin is ideal and Cf switched.

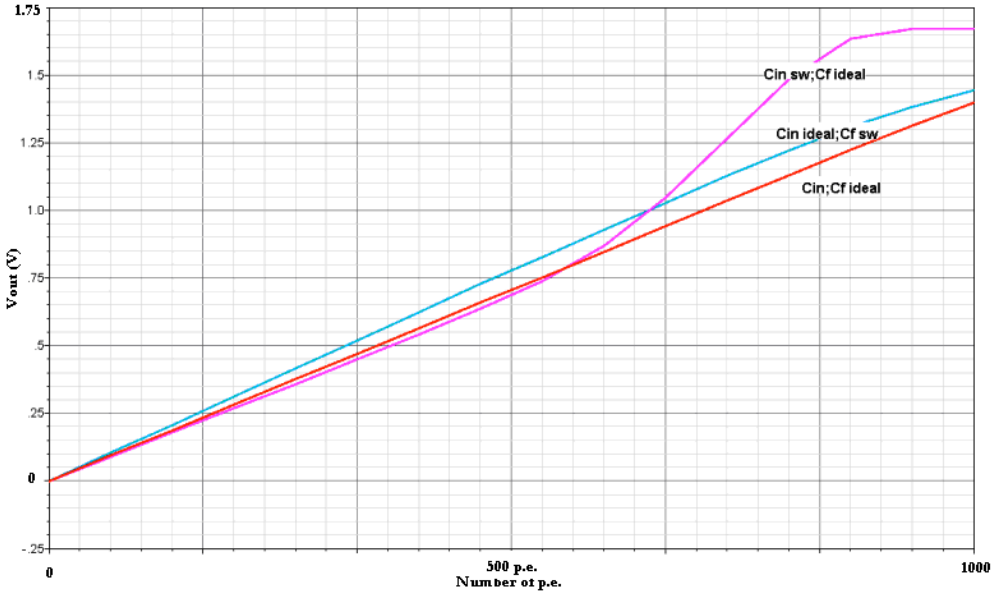

Figure 2.27. Preamplifier linearity for gain 2 (Cin= 1 pF and Cf= 0.5 pF). Pink curve has Cin switched and Cf ideal; the blue curve Cin ideal and Cf switched; the red curve Cin and Cf ideal.

The reason for this strange behavior is due to the input capacitor schematic: closing only one switch, for example 1 pF and opening the others makes the voltage levels (Vx in the Figure 2. 28) for the other capacitances unfixed.

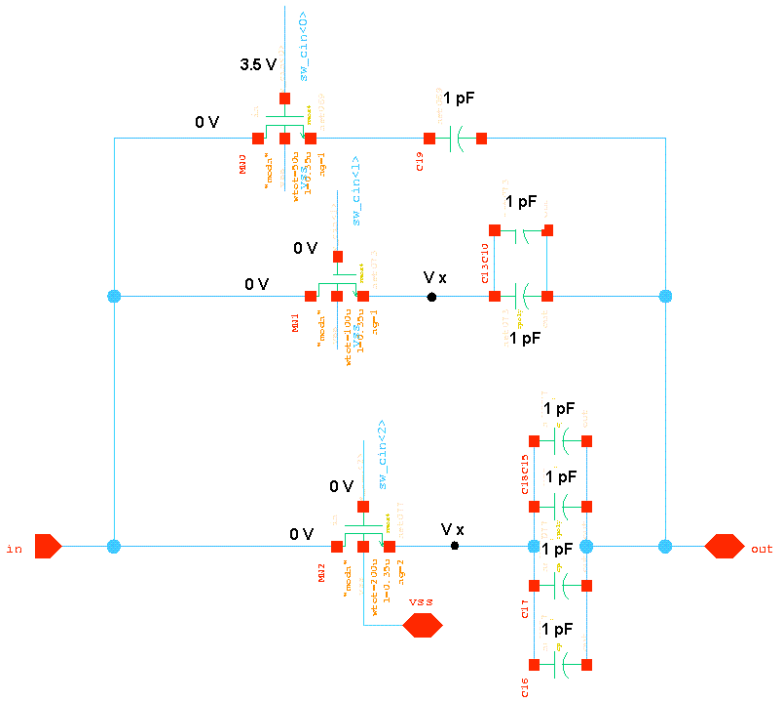

Figure 2. 28. Cin first schematic.

Therefore a large input signal can turn the switch in "on configuration" (VGS>Vt) with an additional injected charge which cannot be evaluated. In order to solve this problem, an additional switch is put in Cin schematic as displayed in Figure 2. 29.

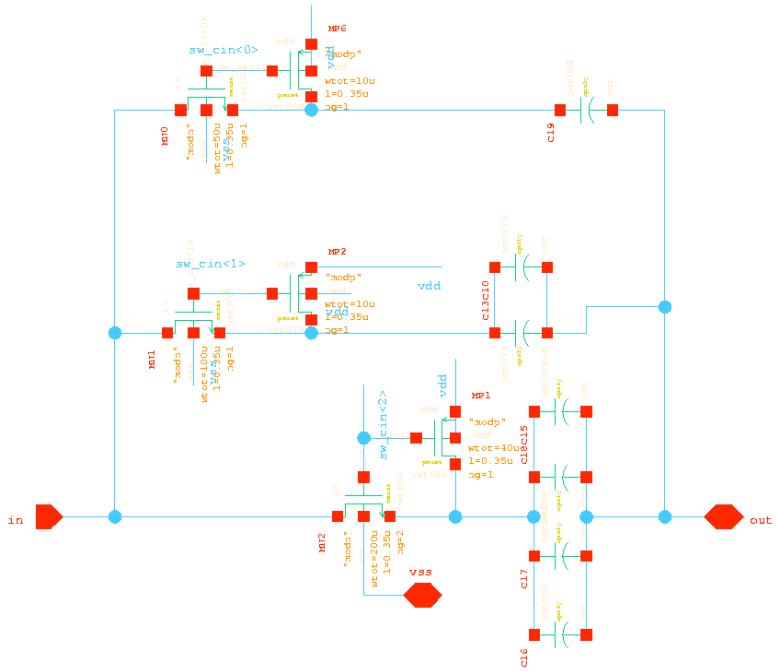

Figure 2. 29. Cin second schematic.

A second, complementary, PMOS switch is added with the gate connected to the NMOS switch gate and the source connected to Vdd. With this structure, when the NMOS switch is in "off configuration" the PMOS switch is in "on configuration" putting the previously Vx value to Vdd. The preamplifier linearity, for small preamplifier gain, in Figure 2.30, shows a better linearity up to 500 p.e. compared to the first linearity results (Figure 2.26).

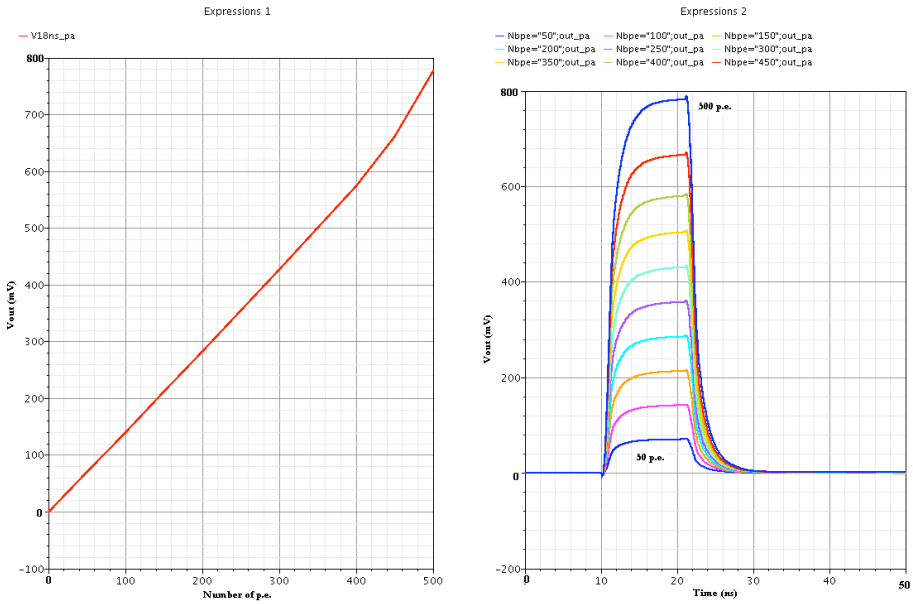

Figure 2.30. Preamplifier linearity for gain 2 (Cin= 1 pF and Cf= 0.5 pF) with 2nd Cin schematic. Left panel the maximum preamplifier value is plotted versus the injected signal until 500 p.e. of current; Right panel the corresponding preamplifier output signals are shown.

The improvements in terms of linearity led to a degradation of the rise time of the output signal.
In Figure 2.31 the rise time change is illustrated adding the other two capacitances in parallel. In the first simulation, the red curve shows the preamplifier output signal for a preamplifier gain of 2 with Cin made only by one capacitance (1 pF) with its switch; in the second simulation (blue curve) the preamplifier has the same gain 2 but in parallel on the 1 pF capacitance is put the 2 pF capacitance with its switch opened; similarly in the third simulation (pink curve), in parallel of 1 pF and 2 pF is put the 4 pF capacitance with its switch opened.
This means that the two other capacitances in parallel, even having the switches opened, introduce parasitic impedances (Figure 2.32).

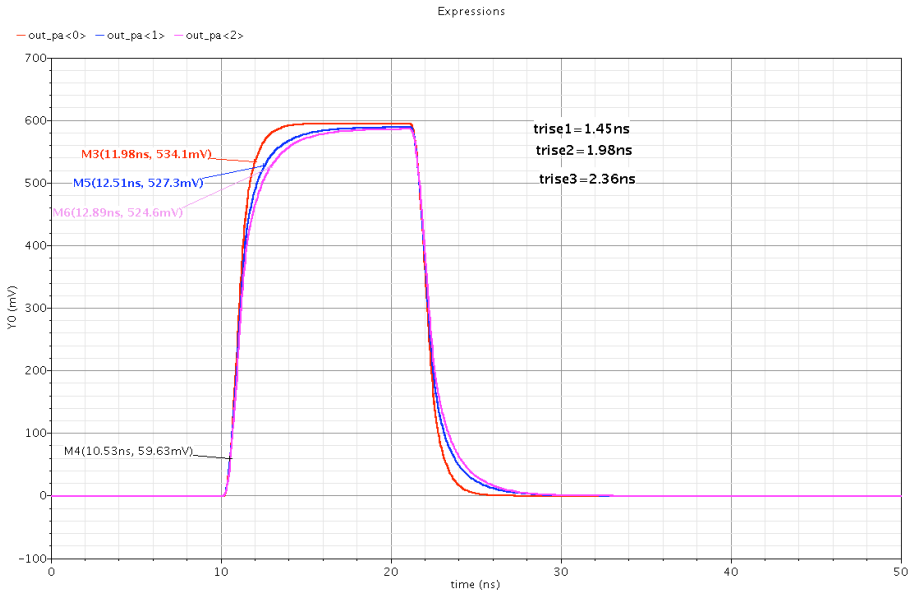

Figure 2.31. Preamplifier output signals at gain 2. Red curve with Cin made only by 1 pF; Blue curve Cin is made by 1 pF in parallel with 2 pF (open switch); Pink curve Cin with 1 pF, 2 pF (open switch) and 4 pF (open switch) in parallel.

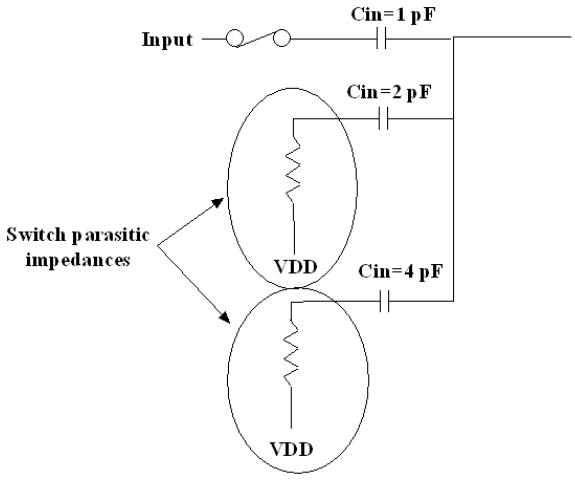

Figure 2.32. Cin parasitic capacitances and resistances.

B. Cf structure

The feedback capacitance Cf has the same structure as Cin but with 8 switched capacitances in parallel. In this case, the choice of the switch has necessitated a PMOS type structure because of the DC levels.

Simulating the preamplifier linearity it has been observed that, for big preamplifier gain (G=8) and for large input signals, the preamplifier output signals have an undershoot (Figure 2.33) due to the switch of the feedback capacitance that, theoretically closed, happens to be opened. This leads to a loss of the charge in the output signal.

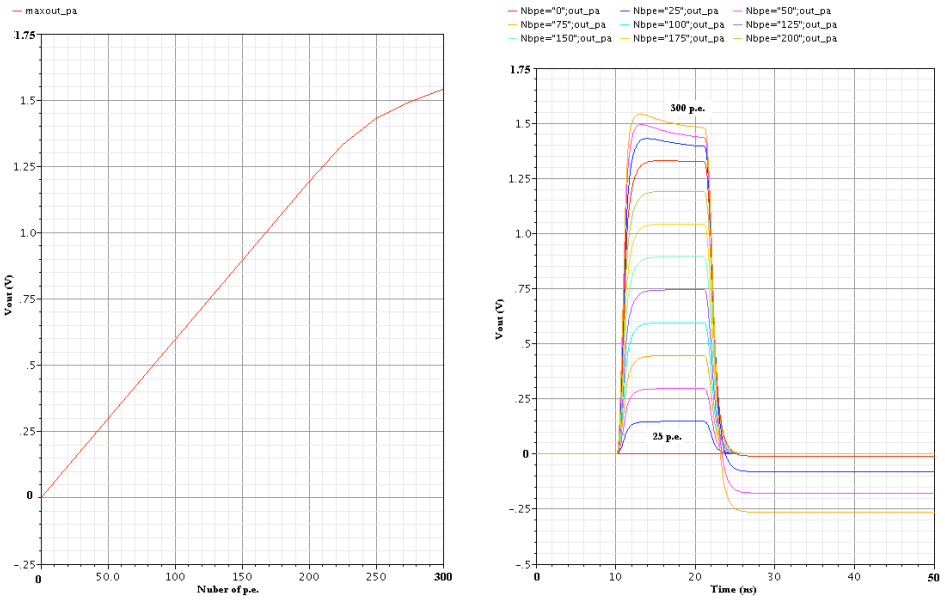

Figure 2.33. Preamplifier linearity for gain 8 (Cin=4 pF and Cf=0.5 pF) with first Cf schematic Left panel the maximum preamplifier value is plotted versus the injected signal until 300 p.e.; Right panel the corresponding preamplifier output signals are shown.

In order to solve this problem, an additional switch is put in Cf schematic as shown in the Figure 2.34.

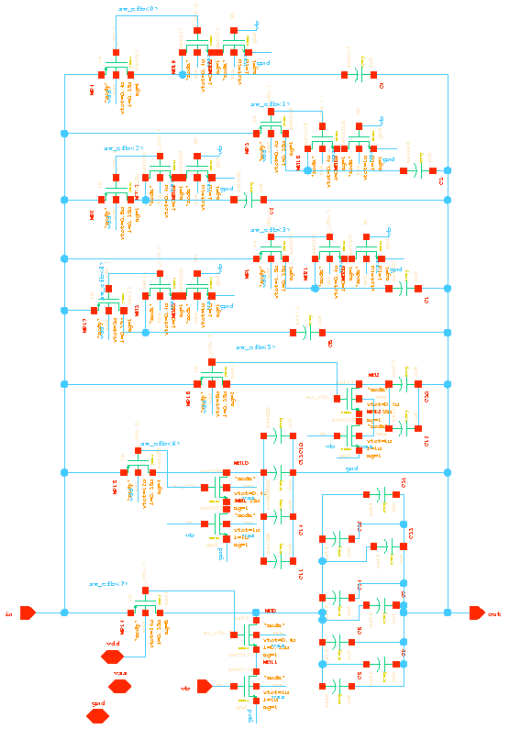

Figure 2.34. Feedback capacitance Cf in the second version.

The second switch (NMOS) is put with the gate connected to the gate of the first PMOS switch so that when the first is opened, the second is closed and the drain is connected to a current source.
The current source injects a charge to compensate the charge lost.

C. Final performances

In the following pictures the preamplifier linearity simulations are shown with Cin and Cf in the new schematics for different gain values. The figures (Figure 2.35, Figure 2.36, Figure 2.37 and Figure 2.38) illustrate the output preamplifier waveforms and the evolution of the maximum value versus the input signal. Good linearity is obtained up to 600 p.e. for small gains and good performances for large gains without undershoots in output signals.

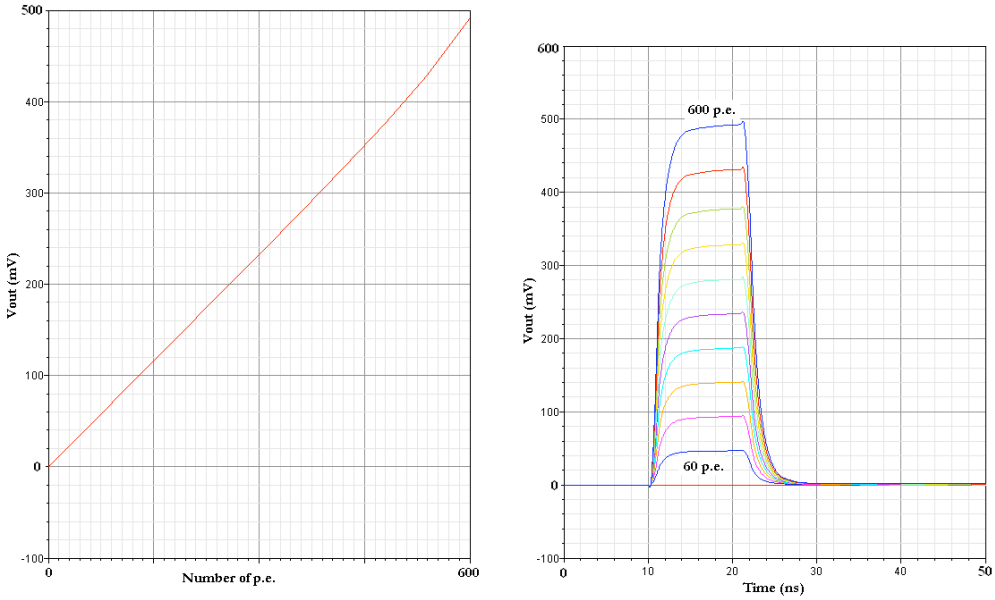

Figure 2.35. Preamplifier linearity simulations. Cin and Cf in the new schematics G(pa)=1.

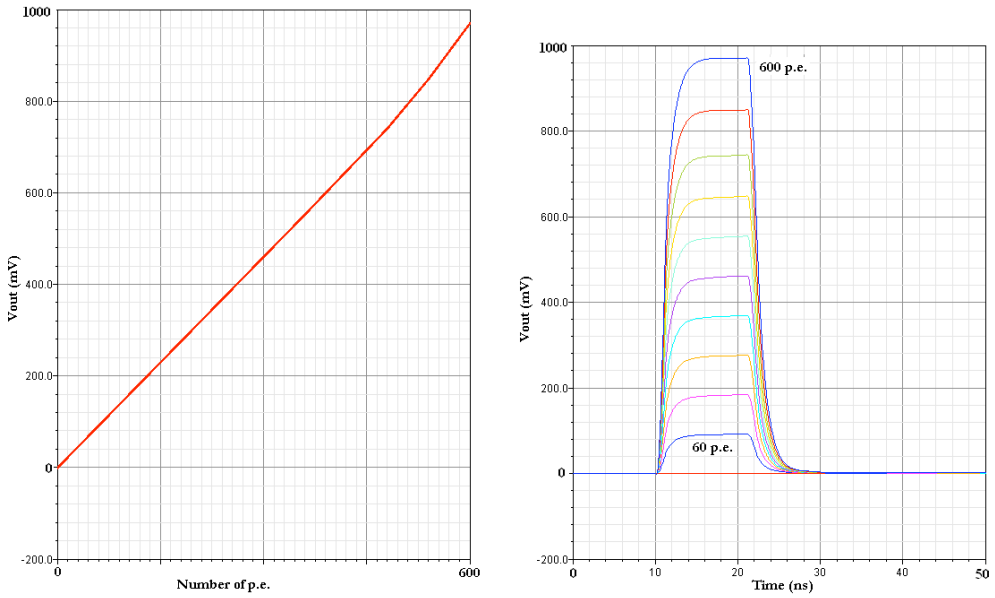

Figure 2.36. Preamplifier linearity simulations. Cin and Cf in the new schematics G(pa)=2.

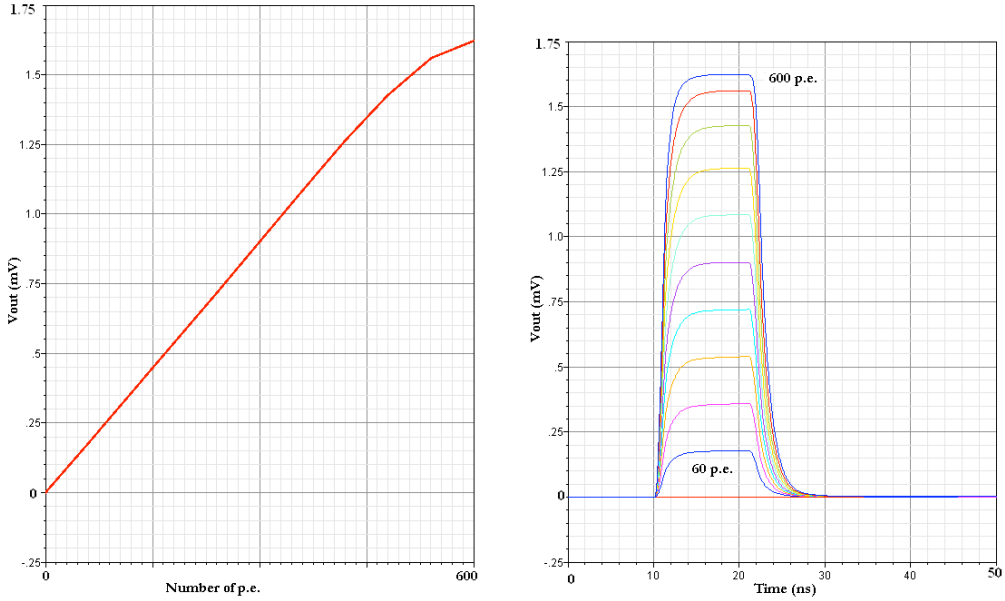

Figure 2.37. Preamplifier linearity simulations. Cin and Cf in the new schematics G(pa)=4.

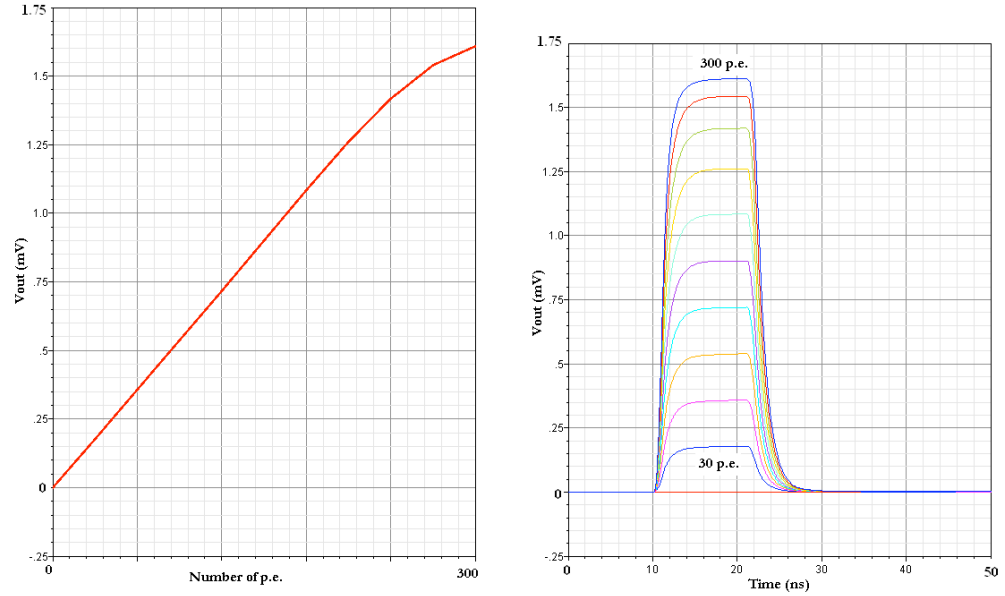

Figure 2.38. Preamplifier linearity simulations. Cin and Cf in the new schematics G(pa)=8.

D. Size of Cin PMOS switch

As it will be detailed in the "Noise section" the preamplifier noise decreased when the width (W) of the PMOS switches is increased.

Increasing transistors W, PMOS noise is reduced (Ron is reduced; $Ron \cong \left[\frac{WC_{ox}}{L}\left(V_{GS}-V_T\right)\right]^{-1}$) and the rise time of the signal is, also, improved (Figure 2.39). The noise simulations listed in Table 2.5 indicate the noise percentage in comparison to the total preamplifier noise for different W PMOS switch values.

W (μm)	Noise (%)
10	17.51
20	9.6
60	3.42
80	2.59

Table 2.5. Noise in % for different W of the Cin PMOS swich.

Figure 2.39 represents the rise time improvement obtained changing the PMOS switch W: the pink and red curves represent the simulation for W= 80 μm and 100 μm; the blue curve, with a bad rise time, represent the simulation for W= 10 μm.
The curves indicate as the rise time is better for bigger PMOS W so by rise time simulations and noise performance on Table 2.5 is chosen a PMOS switch width W= 80 μm.

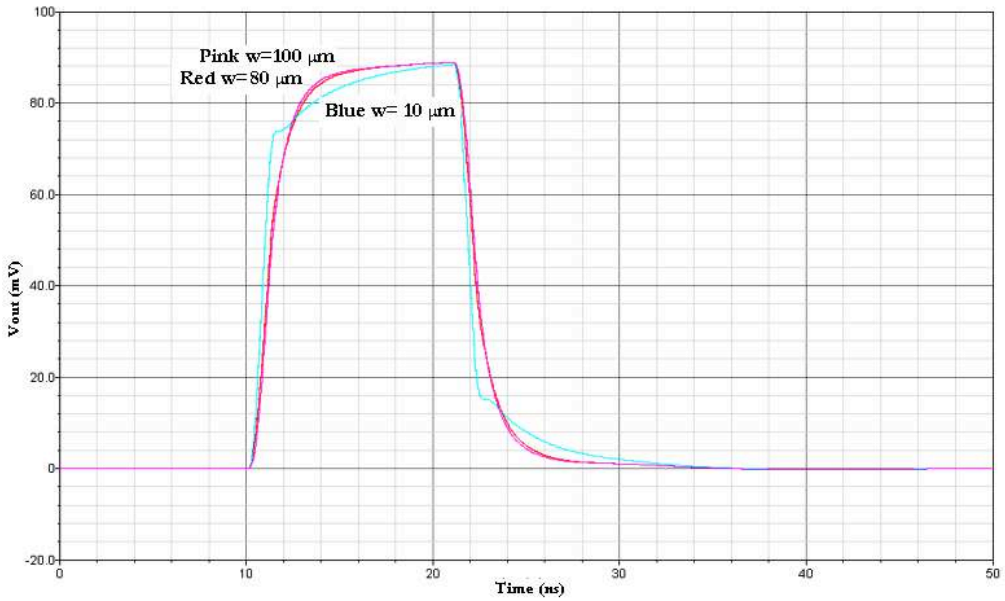

Figure 2.39. Preamplifier output signals for different Cin PMOS W values. Rise time improvements.

3.5. Noise performances

The noise is a relevant characteristic in the preamplifier study; firstly because the first stage noise has a fundamental role on the chip performances and secondly the noise of the other stages has to be negligible. In low noise application the electronic noise is a lower limit for the minimum detectable signal level and also determines the ability of the front-end to distinguish signal levels and measure them precisely [22].
Noise is a totally random signal and it consists of frequency components that are random in amplitude and phase. Although the rms value can be measured, the exact amplitude at any time cannot be predicted. The noise is characterized by statistically. To evaluate the overall effect of the various noise sources for a system with an exact frequency response, it is necessary to know the spectral distribution of the different types of noise. A interesting variable is the *Power spectral density* named *S(ω)* with:

$$S(\omega) = \lim_{T \to \infty} \frac{2V_{nT}(j\omega)}{T} \qquad (2.\ 18)$$

Where T is the time of measurement of $Vn(T)$ *(root mean square or rms)* and $V_{nT}(j\omega)$ *is its Fourier transform*

$$V_n{}^2 = \int_0^\infty S_v(f)df = \frac{1}{2\pi}\int_0^\infty S_v(\omega)d\omega \qquad (2.\ 19)$$

Studying the electronic noise is necessary to describe the noise in terms of voltage and current spectral densities:

$$S_i(f) = \frac{i^2}{\Delta f}\left(\frac{A^2}{Hz}\right) \quad and \quad S_v(f) = \frac{v^2}{\Delta f}\left(\frac{V^2}{Hz}\right) \qquad (2.\ 20)$$

Usually these spectral densities are improperly referred to *en* and *in* with:

$$in = \frac{i}{\sqrt{\Delta f}}\left(\frac{A}{\sqrt{Hz}}\right) \quad \text{and} \quad en = \frac{v}{\sqrt{\Delta f}}\left(\frac{V}{\sqrt{Hz}}\right) \qquad (2.\ 21)$$

The three main types of noise mechanism are referenced as "Thermal noise", "Low frequency noise" and "shot noise" [23].
The "Thermal noise" is caused by the random thermally vibration of the charge carriers in a conductor and is given by the following formula:

$$Sv(f)_{Thermal} = 4kTR\left(\frac{V^2}{Hz}\right) \qquad (2.\ 22)$$

With k= Boltzmann constant and 4kT= $1.66*10^{-20}$ J.

The "Low frequency noise" or "1/f noise" or "Flicker noise" given by the equation 2.23 has as main cause the properties of the surface of the material. The impurity or imperfections in a crystal can trap charge carriers and release them after a characteristic lifetime.

$$Sv(f)_{Flic\,ker} = Kf\,\frac{\Delta f}{f}\left(\frac{V^2}{Hz}\right) \qquad (2.\ 23)$$

The *"Shot noise"* (equation 2.24) is associated to the current that flows across a potential barrier. The probability of a carrier crossing the barrier is independent of any other carriers being emitted, so the individual emissions are random and not correlated.

$$Si(f)_{Shot} = 2qI\left(\frac{A^2}{Hz}\right) \qquad (2.\ 24)$$

Having described these typical source of noise and by the superposition principle, a general electronic component composed by different internal sources of noise can be rapresented by a noiseless component with 2 input noise generators: one voltage noise generator named *series noise (Sv(ω))* and one current noise generator named *parallel noise (Si(ω))* as is shown in Figure 2.40.

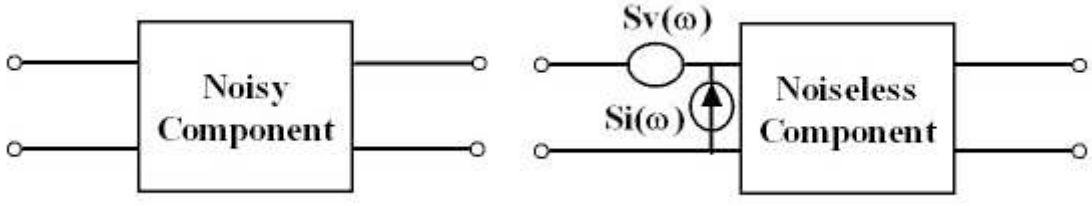

Figure 2.40. Noise generators of a general component.

3.5.1. Preamplifier noise

The preamplifier noise study focuses on:

- Checking that the noise is minimal and is dominated by the input transistor. Therefore to check the 2nd order contributions in order to demonstrate that are negligible;
- Extracting contribution from input Cin switches that can impact the noise.

Considering now the preamplifier general schematic with the series and parallel noise generators, shown in Figure 2.41, the output spectral density is calculated.

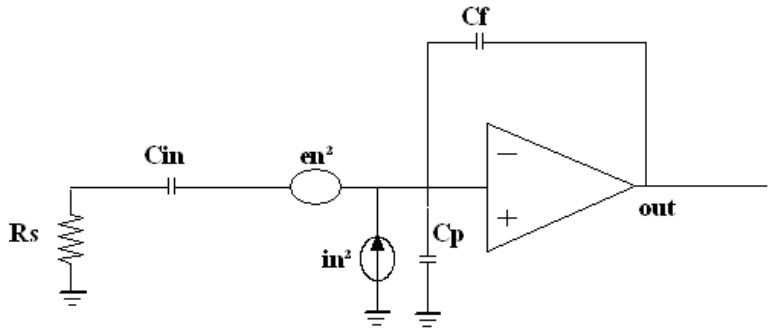

Figure 2.41. Preamplifier input noise generators.

$$Sv_0(\omega) = \left(en^2 + in^2\left|Z_{tot}\right|^2\right) \times \left|H(\omega)_{pa}\right|^2 \qquad (2.\ 25)$$

Where:

- *Ztot* is $Zin + Zp + Rs$ with *Zin* made by the input capacitance Cin (4 pF), *Zp* made by all the parasitic capacitances Cp seen at the preamplifier input and *Rs* the 50 Ω input resistor.
- The frequency response of the preamplifier $H(\omega)_{pa} = \frac{Vout(\omega)}{Vin(\omega)} = -\frac{C_{tot}}{Cf}\left(\frac{1}{1+\frac{j\omega}{\omega_{pa}}}\right)$, with $\omega_{pa} = \frac{G_0\omega_0 Cf}{Cin + Cf}$ and $\omega_0 / 2\pi$ equal to the preamplifier f_{-3dB} frequency.

Supposing $Rs << Zin+Zp$ and named $Ctot = Cin+Cp$: and therefore $\left|Z_{tot}\right| = \left|\frac{1}{j\omega C_{tot}}\right|$

$$Svo(\omega) = \left(en^2 + in^2 \times \left|\frac{1}{j\omega C_{tot}}\right|^2\right)\left|-\frac{C_{tot}}{Cf}\left(\frac{1}{1+\frac{j\omega}{\omega_{pa}}}\right)\right|^2 =$$

$$= \left(en^2\frac{C_{tot}{}^2}{C_f{}^2} + in^2\frac{1}{\omega^2 C_f{}^2}\right)\left(\frac{1}{1+\frac{\omega}{\omega_{pa}}}\right)^2 \qquad (2.\ 26)$$

Considering the preamplifier input series noise source en^2 (supposing parallel noise negligible), the total voltage noise at preamplifier output is given by:

$$Vn^2 = \int_0^\infty en^2 \left|H(\omega)_{pa}\right|^2 \frac{d\omega}{2\pi} = \int_0^\infty \left(en^2 \frac{C_{to}{}^2}{C_f{}^2} \right) \left(\frac{1}{1+\frac{\omega^2}{\omega_{pa}{}^2}} \right) \frac{d\omega}{2\pi} = \int_0^\infty en^2 \frac{C_{tot}{}^2}{C_f{}^2} \left(\frac{1}{1+\frac{\omega^2}{\omega_{pa}{}^2}} \right) \frac{d\omega}{2\pi} =$$

$$\int_0^\infty en^2 \frac{C_{tot}{}^2 \omega^2{}_{pa}}{C_f{}^2} \left(\frac{1}{\omega^2{}_{pa} + \omega^2} \right) \frac{d\omega}{2\pi} = en^2 \frac{C_{tot}{}^2 \omega^2{}_{pa}}{2\pi C_f{}^2} \left[\frac{1}{\omega_{pa}} arctg \frac{\omega}{\omega_{pa}} \right]_0^\infty = \qquad (2.\ 27)$$

$$= en^2 \frac{C_{tot}{}^2 \omega_{pa}}{2\pi C_f{}^2} \frac{\pi}{2} = en^2 \frac{C_{tot}{}^2}{C_f{}^2} \frac{\pi}{2} f_{-3db}$$

Where $f_{-3db} = \frac{\omega_{pa}}{2\pi}$.

The simulation results[42] give the series and parallel noise contributions as displayed in the Figure 2.42. As 1 p.e. (160 fC) gives an output signal of 5.5 mV, the preamplifier rms output noise value of 468 µV corresponds to 13 fC. The Signal to Noise ratio is ~ 12 for the referred signal of 1 p.e. Table 2.6 summarizes the results obtained.

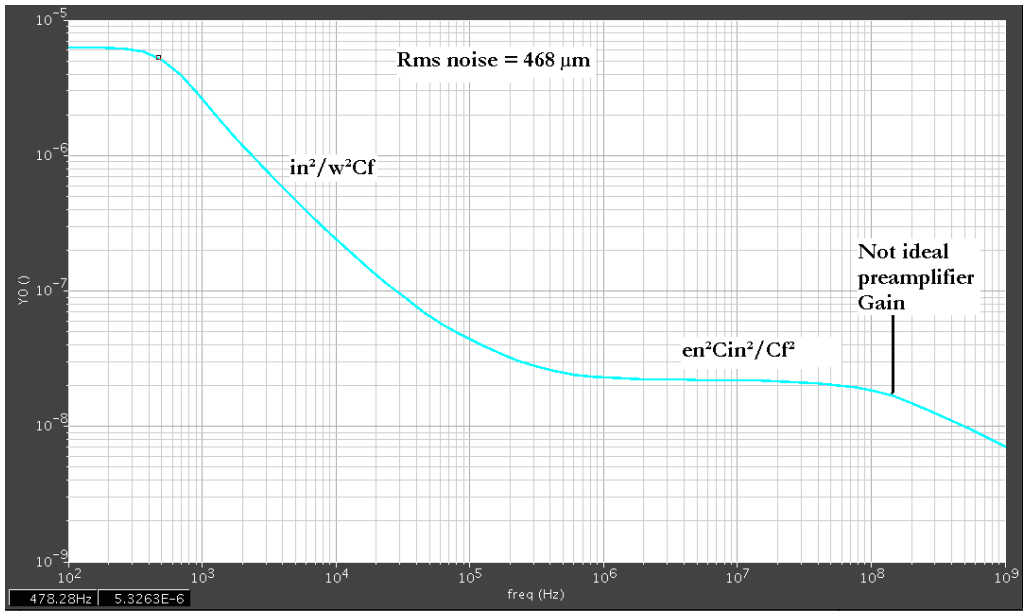

Figure 2.42. Preamplifier noise simulation; Gpa= 8: Cin=4 pF and Cf= 0.5 pF. Root spectral density plot ($\sqrt{Sv_{out}}$).

Rms noise (V)	468uV ~ 1/12 pe ~ 13fC
SNR	12
Vout (1 p.e.) (V)	5.5mV

Table 2.6. Preamplifier noise characteristics.

In order to calculate the series and parallel generators, the noise contribution of each internal component is studied [24]. All the noise sources come from the preamplifier except the thermal noise from Rs (4KTRs) which is in series with the preamplifier series noise and thus adds in quadrature to the preamplifier series noise generator.

[42] The theoretical value will be calculated in the end of the paragraph.

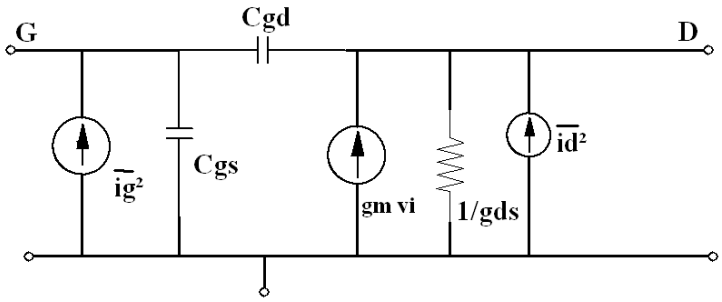

Figure 2.43. MOS noise generators.

The classical sources of noise for a MOS transistor are (Figure 2.43):

1. The shot noise associated with the leakage current Ig:

$$Si(\omega) = 2qIg \qquad (2.\ 28)$$

with q the electron charge.
This parallel source is considered negligible because of the small value of the leakage current ig (~ fA).

2. The thermal noise, due to the thermal motion of the charge carriers in the resistive channel. As in a real resistance, this motion induces a fluctuation of the drain current (*id*). This is represented by a series noise generator:

$$Sv(\omega) = \frac{4KT\alpha}{gm} = \frac{8}{3}\frac{KT}{gm} \qquad (2.\ 29)$$

Typical values for α are: $\alpha = \frac{1}{2}$ in weak inversion; $\alpha = \frac{2}{3}$ for a JFET and $\alpha \cong 1$ in strong inversion. In the following calculations $\alpha = \frac{2}{3}$.
K is the Boltzmann constant 1.38×10^{-23}; gm is the transconductance parameter and T the temperature in °K ($4KT = 1.66*10^{-20}$J).
This drain current fluctuation creates, also, for a capacitive coupling, a gate current fluctuation represented by a parallel generator:

$$Si(\omega) = \frac{\omega^2 Cgs^2}{gm^2}\left(\frac{8}{3}KTgm\right) \qquad (2.\ 30)$$

Where Cgs is the Gate-Source capacitance; typically the small value (~ fF) of this capacitance, squared in the formula (~ 10^{-30}), brought the parallel noise negligible.

3. The 1/f noise is due to the gaps into the crystal and is represented by a series noise:

$$Sv(\omega) = Kf\,\frac{Id^{\alpha}}{\omega^{\alpha}}\,\frac{(2\pi)^{\alpha}}{C_{ox}L_{eff}W_{eff}} \qquad (2.\ 31)$$

Typically $\alpha = 1$ and *Cox* is the capacitance of the oxide layer; *Leff* is effective channel length and *Weff* is effective channel width.
From the parameters given by the AMS datasheet and with α=1, to simplify the calculations:

$$K_{PMOS} = Kf_{PMOS}\frac{1}{C_{ox}L_{eff}W_{eff}} = 1.5\times10^{-11}$$

$$K_{NMOS} = Kf_{NMOS}\frac{1}{C_{ox}L_{eff}W_{eff}} = 2.7\times10^{-11}$$

$$Sv(\omega) = 2\pi K\frac{Id}{\omega} \rightarrow Sv(f) = K\frac{Id}{f} \qquad (2.\ 32)$$

with $K = K_{PMOS}$ or $K = K_{NMOS}$.

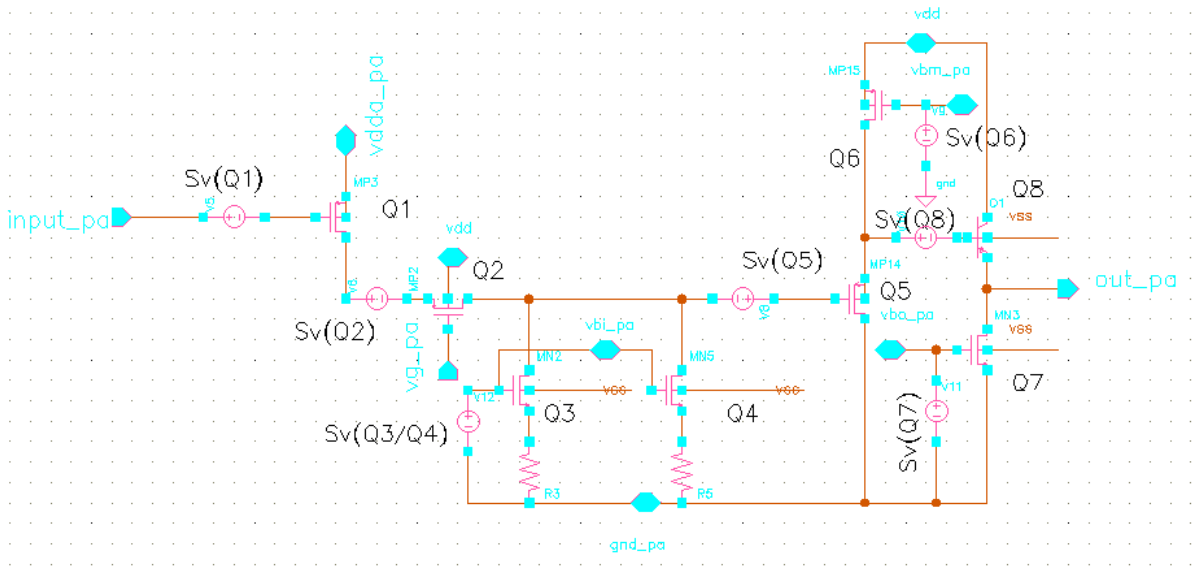

Figure 2.44. Preamplifier noise generators for each internal transistor.

In general, the main sources of noise are: the input transistor Q1 and the current sources Q3 and Q4 (Figure 2.44). This is illustrated also in the preamplifier noise simulation (Figure 2.45) where the main sources of noise are listed at 10 MHz frequency with the noise type, the noise contribution (spectral density in V^2/Hz), and the weight of each contribution in %. The frequency choice (10 MHz) is given by the central frequency value of the filter that follows the preamplifier (§ 4.2 Chapter II).
The simulation results indicate:

- MP1 the input transistor (Q1) with its parallel noise contribution (49.93%);
- R54 the 50 Ω thermal noise (16.52%);
- MP21 the master source of the buffer (Q5) current source with parallel noise contribution (6.61%);
- MN22 the master source of the common base current source (Q3 and Q4) with its 1/f (1.12%) and parallel noise contributions (4.72%);
- MN1 and MN2 the current source transistors with parallel noise contributions (2*2.42%);
- MP14 and MP15 respectively the noise contributions of the input transistor of the buffer (4.37%) and its current source transistor (1.67%).

As explained in the previous calculation, the preamplifier noise is independent from the 50 Ω input resistor (Equation 2.26 and 2.27) and this mean that the input resistor doesn't change the total input equivalent impedence, but this resistor is, however, an important source of noise seen by the simulator in the preamplifier output.
It is important to notice that these results were obtained using ideal input (Cin) and feedback (Cf) capacitances.

Window Expressions Info

Device	Param	Noise Contribution	% Of Total
/MP1	id	1.3418e-16	49.93
/R54	rn	4.43844e-17	16.52
/MP21	id	1.77652e-17	6.61
/MN22	id	1.26806e-17	4.72
/MP14	id	1.17418e-17	4.37
/MN1	id	6.50981e-18	2.42
/MN2	id	6.50981e-18	2.42
/MP15	id	4.4781e-18	1.67
/MN22	fn	3.01035e-18	1.12
/Q1	rbi	1.30292e-18	0.48

Spot Noise Summary (in V^2/Hz) at 10M Hz Sorted By Noise Contributors

Figure 2.45. List of the main preamplifier sources of noise. Simulation results at 10 MHz. with Cin and Cf ideal. Gpa= 8 (Cin= 4 pF and Cf= 0.5 pF).

In simulation a difference in noise results has been observed using ideal or switched input and feedback capacitances.
Figure 2.46 displays this difference: the red curve is the equivalent preamplifier output noise with Cin and Cf in switched structure and values respectively 4 pF and 0.5 pF; the blue curve is the same simulation but with ideal capacitances. A higher rms noise (443 μV) is obtained with the switched capacitance structure as compared to the one with the ideal capacitances (352 μV).

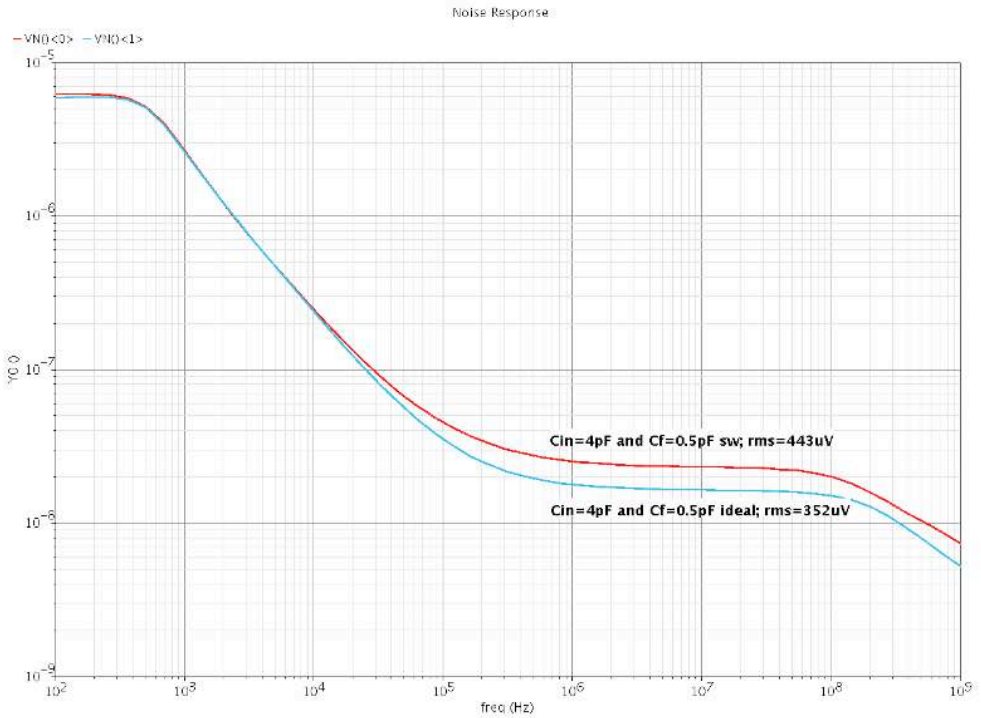

Figure 2.46. Preamplifier noise simulations: red curve for Cin and Cf switched and the blue curve for Cin and Cf ideal, Gpa= 8 (Cin= 4 pF and Cf= 0.5 pF). Root spectral density plot ($\sqrt{Sv_{out}}$).

Figure 2.47 shows the noise component simulations with switched capacitances: noise contributions of the input Cin switch (MP2) and of the feedback switch (MP15) are observed.

Window Expressions Info

Device	Param	Noise Contribution	% Of Total
/MP1	id	3.07612e-16	57.30
/R54	rn	4.26331e-17	7.94
/MN22	id	2.8131e-17	5.24
/MP21	id	1.77518e-17	3.31
/I198/MP2	id	1.54894e-17	2.89
/MN2	id	1.44171e-17	2.69
/MN1	id	1.44171e-17	2.69
/MP14	id	1.1745e-17	2.19
/I199/MP15	id	9.03891e-18	1.68
/MN22	fn	6.67877e-18	1.24

Spot Noise Summary (in V^2/Hz) at 10M Hz Sorted By Noise Contributors

Figure 2.47. List of the main preamplifier sources of noise. Simulation results at 10 MHz with Cin and Cf switched. Gpa= 8 (Cin= 4 pF and Cf= 0.5 pF).

Other results have shown that the noise is unchanged with different input Cin values when the switched structure is used, whereas it changes with ideal Cin values (as expected from the theory). The same result is obtained with measurement (§4 Chapter III).

Supposing the noise sources of each preamplifier internal stages are independent, the total noise source generator referred to the input is given by the squared sum of each contribution.
The contribution of each noise generator is now calculated:

- **The input stage**

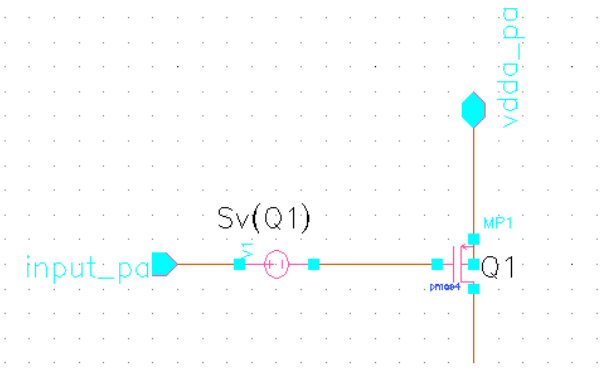

Figure 2.48. Input transistor (Q1) noise generators.

As explained previously and verified in the following calculations, the noise of the input transistor (Figure 2.48) is the main source of the whole chain considering that this extra signal is then amplified by the following stages.
The noise sources for this input transistor are the classical noise generators, shown previously, for a MOS:

$$Sv_1(f) = \frac{8}{3}\frac{KT}{gm_1} + K\frac{Id}{f} \qquad (2.\ 33)$$

With

gm1	Id1
11.13 mA/V	887 µA

Table 2.7. Q1 parameters.

So at 10 MHz:

$$Sv_1(f) = \frac{8}{3}\frac{KT}{gm_1} = 10^{-18}\frac{V^2}{Hz} \qquad (2.\ 34)$$

$$Sv_1(f)\left(1/f\ noise\right) = K_{PMOS}\frac{Id_1}{f} = 1.34\times10^{-21}\frac{V^2}{Hz} \qquad (2.\ 35)$$

then 1/f noise contribution is negligible.
Therefore the input transistor noise is given by the series *id* noise contribution (Equation 2.34) that will be indicated as $Sv_1(f)(Q_1)$.
Using the simulation result and the theoretical calculation can be deduced the total input capacitance (C_{tot}) of the formula:

$$Sv_{out}(f)(Q_1) = 10^{-18}\frac{V^2}{Hz}\times\frac{Ctot^2}{Cf^2} = 1.34\times10^{-16}$$
$$\Rightarrow Ctot = 5.7\,pF \qquad (2.\ 36)$$

This capacitance is given by: $Ctot = Cin + Cf + Cpa$ where Cpa is the preamplifier input parasitic capacitance given by the input transistor.
Then $Cpa = Ctot - Cin - Cf = 1.2\,pF$; a theoretical calculation demonstrates that a transistor has around 5 fF/μm² of parasitic capacitance (C_{GD} plus C_{GS}). Thus for the preamplifier input transistor with a length of 0.35 μm and a width of 800 μm the parasitic capacitance is around 1.4 pF in agreement with the simulation result.
Recalculating the *Ctot* value with the $S_{vout}(f)$ obtained in simulation with the switched *Cin* the value is different:

$$Sv_{out}(f)(Q_1) = 10^{-18}\frac{V^2}{Hz}\times\frac{Ctot^2}{Cf^2} = 3.08\times10^{-16}$$
$$\Rightarrow Ctot = 8.7\,pF \qquad (2.\ 37)$$

This can be seen by the picture (Figure 2.49): the two other input capacitances, 2 pF and 1 pF, are connected to the preamplifier input by the switch *Ron* value to Vdd. In fact $Ctot = Cin + Cf + Cpa + Cin_{2\,pF} + Cin_{1\,pF} = 5.7\,pF + 1pF + 2\,pF = 8.7\,pF$ exactly the value calculated above.

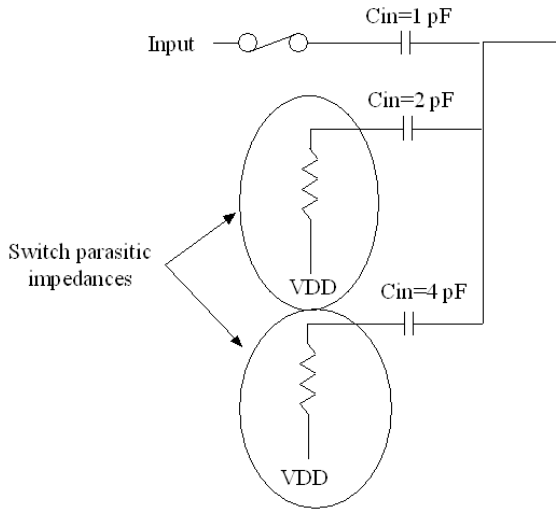

Figure 2.49. Input Cin capacitance equivalent schematic.

The contribution at the preamplifier noise of the other stages is theoretically negligible. This will be verified in the following calculations.

- **Second stage**

The second stage is described by Figure 2.50 and its transistor parameters are given by Table 2.8.

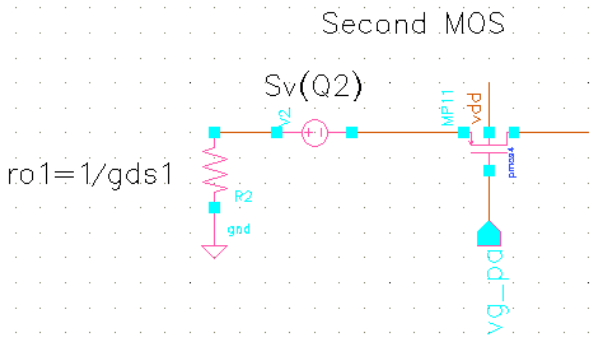

Figure 2.50. Second transistor (Q2) noise generator.

gm2	Id2
4.2 mA/V	887 µA

Table 2.8. Q2 parameters.

The noise of the second stage is at 10 MHz:

$$Sv_2(f) = \frac{8}{3}\frac{KT}{gm_2} = 2.6\times10^{-18}\frac{V^2}{Hz} \qquad (2.\ 38)$$

Then the series noise is transformed to a current noise by to $r_{o1} = \frac{1}{gds_1}$ and is referred to the preamplifier input by dividing by gm_1^2.

$$Sv_2(f)(Q_2) = \frac{Sv_2}{r_{o1}^2 gm_1^2} \qquad (2.\ 39)$$

As $r_{o1} = \frac{1}{gds_1}$ and gds = 390 µA/V ; gm_1 = 11.13 mA/V :

$$Sv_2(f)(Q_2) = \frac{Sv_2}{r_{o1}^2 gm_1^2} = Sv_2\left(\frac{gds_1}{gm_1}\right)^2 \cong 3\times10^{-21}\frac{V^2}{Hz} \qquad (2.\ 40)$$

The second transistor has the same current Id_2 as the input transistor, the same 1/f parameter K_{PMOS} and so the 1/f noise contribution has the same value:

$$Sv_2(f)\left(\frac{1}{f}\,noise\right) = K_{PMOS}\frac{Id_2}{f} = K_{PMOS}\frac{Id_1}{f} = 1.34\times10^{-21}\frac{V^2}{Hz} \qquad (2.\ 41)$$

But this noise is referred to the input by:

$$Sv_2(f)(Q_2) = Sv_2(f)(1/f\ noise)\left(\frac{gds_1}{gm_1}\right)^2 = 1.64\times10^{-24}\frac{V^2}{Hz} \qquad (2.\ 42)$$

- **The current source**

The current source is represented in Figure 2.51 and the transistor parameters are listed in Table 2.9.

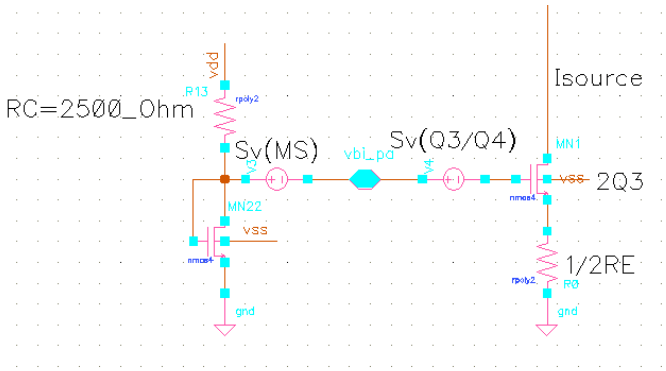

Figure 2.51. Current source noise generators.

gm_{MS}	**Id_{MS}**	**RC**
1.7 mA/V	849 µA	2500 Ω
gm3	**Id3**	**RE**
1.3 mA/V	441 µA	500 Ω

Table 2.9. Current source parameters.

The master source noise generators are (10 MHz):

$$Sv(f)(R_C) = \frac{4KT}{R_C gm^2{}_{MS}} = 2.2\times10^{-18}\frac{V^2}{Hz} \qquad (2.\ 43)$$

$$Sv(f)(MS) = \frac{8KT}{3gm_{MS}} = 6.4\times10^{-18}\frac{V^2}{Hz} \qquad (2.\ 44)$$

$$Sv(f)\left(1/f\right)(MS) = K_{NMOS}\frac{Id(MS)}{f} = 2.3\times10^{-21}\frac{V^2}{Hz} \qquad (2.\ 45)$$

The two transistors in parallel are simplified as a single one with a double size and a degenerated equivalent resistor equal to ½ R_E.

The noise generators, in this case, are:

$$Sv(f)(Q3/Q4) = 2\frac{4KT}{3gm_3} = 10^{-17}\frac{V^2}{Hz} \qquad (2.\ 46)$$

$$Sv(f)\left(1/f\ noise\right)(Q3/Q4) = K_{NMOS}\frac{2Id(Q3)}{f} = 2.4\times10^{-21}\frac{V^2}{Hz} \qquad (2.\ 47)$$

These series noise generators are converted in parallel one and then referred to the preamplifier input.

$$Sv(f)(currentsource) = \frac{Sv}{gm_1{}^2}\left(\frac{gm_3}{1+gm_3\frac{R_E}{2}}\right)^2 \qquad (2.\ 48)$$

As the source is degenerated by ½ R_E, gm is replaced by:

$$gm_3 \rightarrow \left(\frac{gm_3}{1+gm_3\frac{R_E}{2}}\right) \qquad (2.\ 49)$$

Therefore we obtain at 10 MHz:

$$Sv(f)(Mastersource) = 5\times10^{-20}\,\frac{V^2}{Hz}$$

$$Sv(f)(Q3/Q4) = 10^{-19}\,\frac{V^2}{Hz}$$

$$Sv(f)(\tfrac{1}{f}\,noise)(Mastersource) = 1.8\times10^{-23}\,\frac{V^2}{Hz}$$

$$Sv(f)(\tfrac{1}{f}\,noise)(Q3/Q4) = 1.9\times10^{-23}\,\frac{V^2}{Hz}$$

- **The output buffer**

The output buffer is displayed in Figure 2.52 and the transistors parameters are listed in Table 2.10.

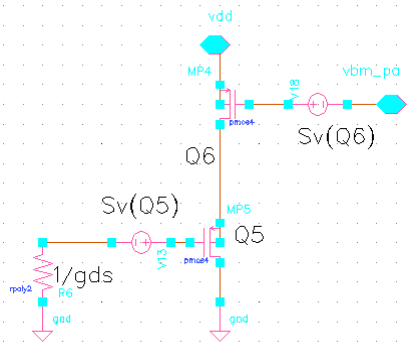

Figure 2.52. Output buffer noise generators.

gm5	Id5
1.1 mA/V	111 µA
gm6	**Id6**
417 µA/V	113 µA

Table 2.10. Output buffer parameters.

The noise generators of Q5 are (10 MHz):

$$Sv_5(f) = \frac{8}{3}\frac{KT}{gm_5} = 10^{-17}\,\frac{V^2}{Hz} \qquad (2.\ 50)$$

$$Sv_5\left(f\right)\left(\tfrac{1}{f}\,noise\right) = K_{PMOS}\,\frac{Id_5}{f} = 1.7\times10^{-22}\,\frac{V^2}{Hz} \qquad (2.\ 51)$$

These are changed in current multiplying Sv by 1/gds3 and then referred to the preamplifier input by:

$$Sv_2(f)(Q_5) = Sv_5\left(\frac{2gds3}{gm_1}\right)^2 \cong 2\times10^{-22}\,\frac{V^2}{Hz} \qquad (2.\ 52)$$

$$Sv(f)\left(\tfrac{1}{f}\,noise\right)(Q_5) = Sv_5\left(\tfrac{1}{f}\,noise\right)\left(\frac{2gds3}{gm_1}\right)^2 \cong 3\times10^{-27}\,\frac{V^2}{Hz} \qquad (2.\ 53)$$

With *gds3 =gds (Q3 or Q4)* = 24 µA/V.

For the current source represented in Figure 2.53 with gm_{MSb}= 81 µA/V and Id_{MSb}=22 µA:

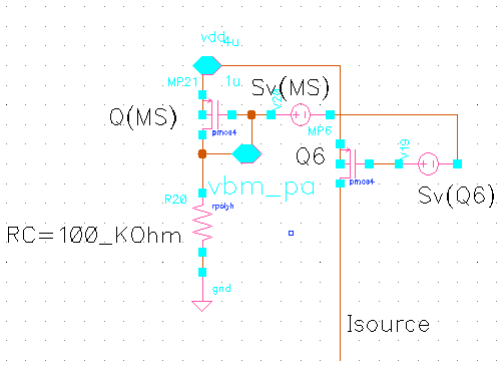

Figure 2.53. Current source noise generators.

$$\begin{aligned}
&Sv(f)(MSb) = \frac{8KT}{3gm_{MSb}} + \frac{4KT}{R_C\,gm^2{}_{MSb}} = 10^{-16}\,\frac{V^2}{Hz}\\
&Sv(f)\left(\tfrac{1}{f}\,noise\right)(MSb) = K_{PMOS}\,\frac{Id(MS)}{f} = 3.3\times10^{-23}\,\frac{V^2}{Hz}\\
&Sv(f)(Q6) = \frac{8KT}{3gm_6} = 1.3\times10^{-17}\,\frac{V^2}{Hz}\\
&Sv(f)\left(\tfrac{1}{f}\,noise\right)(Q6) = K_{PMOS}\,\frac{Id(Q6)}{f} = 1.71\times10^{-22}\,\frac{V^2}{Hz}
\end{aligned} \qquad (2.\ 54)$$

In preamplifier input:

$$Sv(f) \rightarrow Sv(f)\left(\frac{gm_6}{gm_5}\times\frac{2gds_3}{gm_1}\right)^2 \qquad (2.\ 55)$$

and $\left(\frac{gm_6}{gm_5}\times\frac{2gds_3}{gm_1}\right)^2 = 2.6\times10^{-6}$

So at 10 MHz:

$$Sv(f)(MSb) = 2.6\times10^{-22}\,\frac{V^2}{Hz}$$

$$Sv(f)(\tfrac{1}{f}\,noise)(MSb) = 8\times10^{-29}\,\frac{V^2}{Hz}$$

$$Sv(f)(Q6) = 3.4\times10^{-23}\,\frac{V^2}{Hz}$$

$$Sv(f)(\tfrac{1}{f}\,noise)(Q6) = 4.4\times10^{-28}\,\frac{V^2}{Hz}$$

To conclude, the contributions of each stage are listed in the following table:

Sv(f) (Q_1)	**Sv(f) (Q_2)**	**Sv(f) (Q_3/Q_4)**	**Sv(f) (Q_{MS})**
$10^{-18}V^2/Hz$	$3*10^{-21}$ V^2/Hz	10^{-19} V^2/Hz	$5*10^{-20}$ V^2/Hz
Sv(f) (Q_5)	**Sv(f) (Q_6)**	**Sv(f) (Q_{MSb})**	
$2*10^{-22}$ V^2/Hz	$3.4*10^{-23}$ V^2/Hz	$2.6*10^{-22}$ V^2/Hz	
Sv(1/f) (Q_1)	**Sv(1/f) (Q_2)**	**Sv(1/f) (Q_3/Q_4)**	**Sv(1/f) (Q_{MS})**
$1.3*10^{-21}$ V^2/Hz	$1.64*10^{-24}$ V^2/Hz	$1.9*10^{-23}$ V^2/Hz	$1.8*10^{-23}$ V^2/Hz
Sv(1/f) (Q_5)	**Sv(1/f) (Q_6)**	**Sv(1/f) (Q_{MSb})**	
$3*10^{-27}$ V^2/Hz	$4.4*10^{-28}$ V^2/Hz	$8*10^{-29}$ V^2/Hz	

Table 2.11. Preamplifier noise source generators.

The total input voltage noise contribution is given by the sum of each contribution:

$$Sv_{tot}(f) = Sv(f)(Q_1) + Sv(f)(Q_2) + Sv(f)(Q_3/Q_4) + Sv(f)(Q_{MS}) + Sv(f)(Q_5) + Sv(f)(Q_6) + Sv(f)(Q_{MSb}) +$$
$$Sv(f)\left(\tfrac{1}{f}\,noise\right)(Q_1) + Sv(f)\left(\tfrac{1}{f}\,noise\right)(Q_2) + Sv(f)\left(\tfrac{1}{f}\,noise\right)(Q_3/Q_4) + Sv(f)\left(\tfrac{1}{f}\,noise\right)(Q_{MS}) +$$
$$Sv(f)\left(\tfrac{1}{f}\,noise\right)(Q_5) + Sv(f)\left(\tfrac{1}{f}\,noise\right)(Q_6) + Sv(f)\left(\tfrac{1}{f}\,noise\right)(Q_{MSb}) \cong 10^{-18}\,\frac{V^2}{Hz}$$

3.5.2. OTA feedback

As explained previously, the preamplifier feedback is made from a capacitance (Cf) and an OTA. The capacitance is noiseless but the OTA adds to the preamplifier input a parallel noise contribution. The OTA output is connected to the preamplifier input so its parallel noise is injected in the preamplifier input. The output parallel noise has been calculated from the series noise contribution of each stages (Figure 2.54) using *gm1= gm2= gm3= gm4=* 11.3 nA/V; *gm5= gm6= gm7= gm8=* 1.4 µA/V; gm9= 21.3 nA/V.

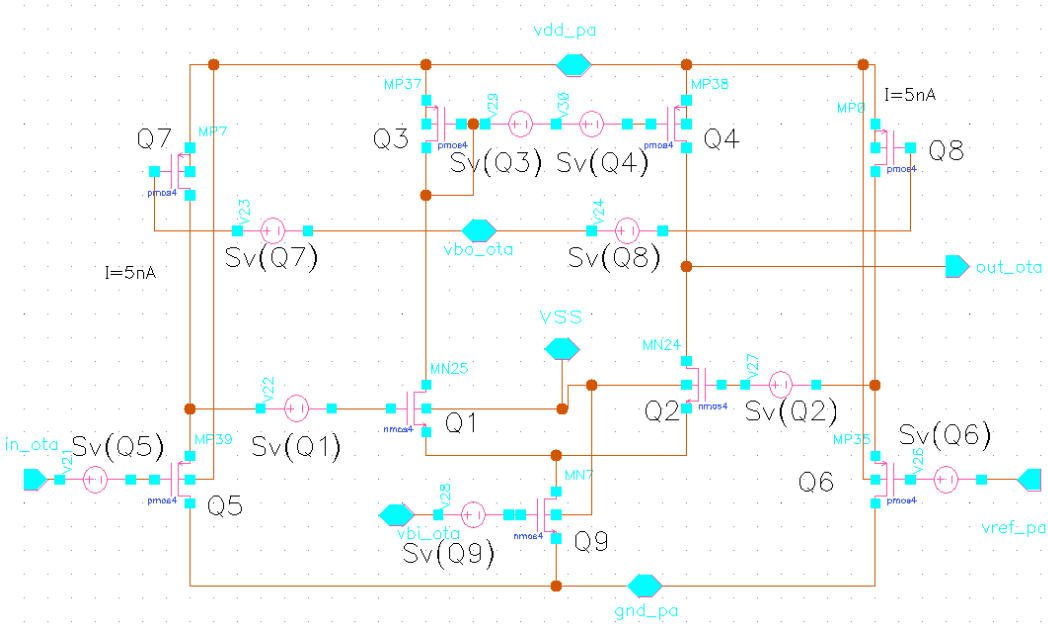

Figure 2.54. Feedback OTA noise generators.

Supposing that the parallel noise and the 1/f noise of each transistor are negligible:

- The transistor Q1 has an input series noise $Sv_1(\omega)$ which is transformed in current noise multiplying by gm_1 : $Si_1(\omega) = Sv_1(\omega) \times gm_1^2$;
- For Q2 : $Si_2(\omega) = Sv_2(\omega) \times gm_2^2$;
- For Q3 and Q4: $Si_3(\omega) = Sv_3(\omega) \times gm_3^2$ and $Si_4(\omega) = Sv_4(\omega) \times gm_4^2$.

For each transistor the series noise is $Sv(f) = \frac{8}{3}\frac{KT}{gm}$ and with *gm1= gm2= gm3= gm4* thus $Sv_1(f) = Sv_2(f) = Sv_3(f) = Sv_4(f) = \frac{8}{3}\frac{KT}{gm_1}$ which corresponds to a noise of $Si(f) = 4Sv_1(f) \times gm_1^2$ at the OTA output.
The transistor Q5 exhibits an input noise generator $Sv_5(f)$. Q5 is a follower so the voltage noise is brought directly to the input of Q1 and then, as above, transformed in current noise at the Ota output. As for Q6, Q7, Q8.
Therefore at the OTA output, Q5, Q6, Q7 and Q8 give a noise of $Si(f) = 4Sv_5(f) \times gm_1^2$ with $Sv_5(f) = Sv_6(f) = Sv_7(f) = Sv_8(f) = \frac{8}{3}\frac{KT}{gm_5}$.

The transistor Q9 has an input noise of $Sv_9(f) = \frac{8}{3}\frac{KT}{gm_9}$, transformed in current by: $Si_9(f) = \frac{8}{3}\frac{KT}{gm_9} \times gm_9^2$.

To summarized:

$$Si_{tot}(f) = 4\frac{8}{3}\frac{KT}{gm_1} \times gm_1^2 + 4\frac{8}{3}\frac{KT}{gm_5} \times gm_1^2 + \frac{8}{3}\frac{KT}{gm_9} \times gm_9^2 = 7 \times 10^{-28}\ \frac{A^2}{Hz} \qquad (2.\ 56)$$

3.5.3. Total preamplifier output noise

From the calculations presented in the previous sections, we get:

- The parallel noise injected by the feedback OTA with $Si_{tot}(f) = en^2 = 7 \times 10^{-28}\ \frac{A^2}{Hz}$;
- The series noise given from the preamplifier input stage and the input resistor Rs with

$$Sv_{tot}(f) = en^2 = en^2{}_{PA} + en^2{}_{R_S} = 10^{-18}\ \frac{V^2}{Hz} + 4KTRs = 10^{-18}\ \frac{V^2}{Hz} + 8.3*10^{-19} = 1.83*10^{-18}$$

$$Svout(f) = \left(\frac{en^2}{\frac{1}{(2\pi f)^2 Ctot^2}} + in^2 \right) \frac{1}{(2\pi f)^2 Cf^2} = \frac{in^2}{(2\pi f)^2 Cf^2} + \frac{en^2 Ctot^2}{Cf^2} =$$

$$= \frac{Si_{tot}(f)}{(2\pi f)^2 Cf^2} + Sv_{tot}(f)\frac{Ctot^2}{Cf^2} = \qquad (2.\ 57)$$

$$= \frac{7 \times 10^{-28}\ A^2/Hz}{(2\pi f)^2 (0.5\,pF)^2} + \frac{1.83 \times 10^{-18}\ V^2/Hz\ (8.7\,pF)^2}{(0.5\,pF)^2} \approx$$

$$\approx (at\_10MHz) 7.32 \times 10^{-16}\ V^2/Hz$$

Calculating now the rms noise value by: $Vn^2 = en^2 \frac{C_{in}{}^2}{C_f{}^2}\frac{\pi}{2} f_{-3db}$

With:

$f_{-3db} = \frac{\omega pa}{2\pi} = 300MHz$ and $\omega pa = \frac{G_0 \omega_0 Cf}{Cin + Cf}$, G_0= 265, ω_0= $2\pi f_0$, f_0= 10 MHz,

Cf= 0.5 pF

Cin= *Ctot*= *Cin*+*Cparas*= 8.7 pF,

en^2= 10^{-18} V^2/Hz the

The *Vn* value is 374μV (simulation value 468μV) in relative good agreement with the simulation results.

3.6. Conclusion

The input stage of the chip has been analyzed dividing its structure in three main components:

- The preamplifier;
- The input and feedback capacitances (Cin and Cf);
- The OTA in feedback.

The preamplifier is a fast voltage preamplifier with bandwidth of ~ 1.5 GHz. The study of the stability indicates that it will have a stable behavior. The output rms noise attended will be of ~ 500 μV. The 1 p.e. output signal has an amplitude of 5.5 mV (at gain 8) and its linearity study indicates good performances until 300 p.e. (the dynamic range required).
The switched capacitance structures have been studied in order to optimize its behavior in terms of linearity. A dependence of the noise performances by the Cin is expected in the phase of measurements.

4. Signal processing

The purpose of the ASIC is the charge and the time measurement. After a first amplification, the detector signal must be processed to perform measurements (charge and time).
To optimize these two measurements and in particular to optimize the Signal to noise Ratio (SNR), a shaper is needed after the preamplifier.
The analysis of pulse shaper involves three steps:

1. Determine the pulse amplitude for a known impulse charge;
2. Evaluate the total noise at the shaper output;
3. From signal-to-noise ratio (SNR) extrapolate the input charge that gives a SNR of one. This is the equivalent noise charge.

4.1. Quantity for noise measurements

The preceding section has expressed noise in terms of voltage or current spectral density.
Rather than specifying the noise in absolute terms, it is often more useful to express it in terms of the quantity to be measured as the Equivalent Noise Charge (ENC) or Signal to Noise Ratio (SNR) [23].
Readout systems that measure signal charge can be characterized in terms of ENC, i.e. the signal charge that yields a SNR of one.
If the input charge is Qs the ENC is:

$$ENC = Qn = \frac{Qs}{SNR} \qquad (2.\ 58)$$

ENC is commonly expressed in fC or unit of electronics charge e= $1.602*10^{-19}$ C.
If the SNR is expressed as the ratio between the magnitude of the output voltage signal Vs, for the known input charge Qs, and the output rms noise value is Vn, the ENC is given by:

$$ENC = Qn = \frac{Qs \times Vn}{Vs} \qquad (2.\ 59)$$

4.2. Slow Shaper

The slow shaper is an important part of the ASIC. It has three main functions:

- Optimize the SNR (has explained in the introduction of the section);
- Shape the preamplifier signal in order to allow the charge measurements;
- Add a stage of amplification.

In this sub-section the shaper will be studied and will be simulated its performances.

The signal fluctuations, induced by the electronic noise, in the preamplifier output are reduced by the shaper (a filter *H(s)*) placed at the preamplifier output.
The *Optimum Filter H(s)* is that allows to maximize at *tm* (the time of measurement) the *Signal to Noise Ratio* (SNR).
It is well known that the signal to noise ratio of preamplifiers is improved by increasing the number of integration in the shaper using a CRRC^n: the low-pass filter $(RC)^n$ increases the rise time to limit the noise bandwidth and cuts off the high frequency noise; the high-pass filter (CR) cuts the parallel noise.
In PARISROC ASIC, as well as many other ASICs, is used a shaper CRRC² (Figure 2.55) with variable time constant τ=RC.

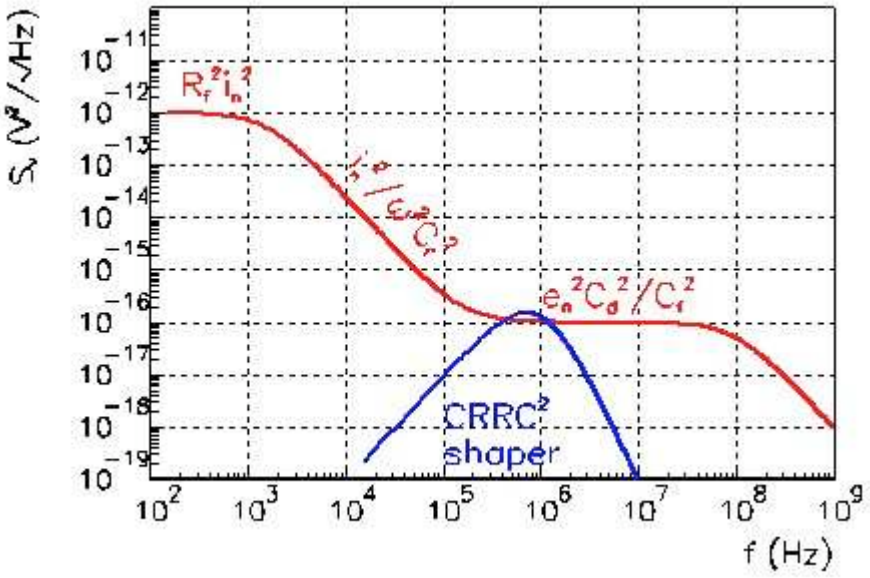

Figure 2.55. Example of CRRC²shaper noise spectral density.

The transfer function for a CRRC² is:

$$H(s) = \frac{\tau s}{(1+\tau s)^3} \qquad (2.\ 60)$$

With central frequency located at $fc = \frac{1}{2\pi\tau\sqrt{2}}$ and $\tau = RC$.

The preamplifier cannot be considered ideal so it contributes to the signal shaping and its transfer function can be approximated by:

$$Hpa(s) = \frac{Cin}{Cf\left(1+\tau_{pa}\right)} \qquad (2.\ 61)$$

With τ_{pa}= 6 ns (simulation result).
From the transfer function, we can calculate the response of the overall chain to an injected charge of Q0δ(t) (dirac pulse), by taking the inverse Laplace transform [25].

$$V_{\delta}(t) = L^{-1}\left[Qo \times H_{pa}(s) \times H_{sh}(s)\right] = Qo\frac{Cin}{Cf}\frac{1}{\tau}h(t) \qquad (2.\ 62)$$

That gives at filter output the following response:

$$h(x) = \left[\frac{x^2}{2} + \frac{x}{\lambda - 1} + \frac{\lambda}{(\lambda+1)^2}\right]\frac{e^{-x}}{\lambda - 1} - \frac{\lambda e^{-x/\lambda}}{(\lambda-1)^3} \qquad (2.\ 63)$$

Putting $x = \frac{t}{\tau}$ and $\lambda = \frac{\tau_{pa}}{\tau}$, for $\lambda = 0$ so $\tau_{pa} = 0$ and for an ideal Dirac delta, the time response of the shaper is:

$$h(t) = \frac{(2-x)}{2\tau}xe^{-x} \qquad (2.\ 64)$$

With:

$t_{\max} = \max\_time = 0.56\tau$

$V_{\max} = \max\_voltage = \frac{0.2306}{\tau}$

$tp = peaking\_time = 1.82\tau$

In the following table are listed the maximum amplitudes, the peak position and the peaking time for different λ values.

λ=τpa/τ	hmax	tmax/τ	tp/τ
0	0.2306	0.586	0.574
0.2	0.2136	0.816	0.744
0.5	0.1740	1.053	0.951
1	0.1306	1.268	1.144
1.5	0.1045	1.395	1.259
2	0.0873	1.482	1.338
3	0.0657	1.594	1.441

Table 2.12. Maximum amplitudes, the peak position and the peaking time for different λ values for an injected Dirac pulse.

The rms noise, due to the preamplifier, at the shaper output is obtained by multiplying the output noise spectral density (Equation 2.26) by the module of the shaper transfer function (Equation 2.60) and integrating over the whole frequency spectrum:

$$Vn^2 = \int Sv(\omega)\left|H(\omega)\right|^2\frac{d\omega}{2\pi} = \frac{en^2Ctot^2}{Cf^2}\frac{1}{\tau}Ia(2) + \frac{in^2}{Cf^2}Ib(2)\tau \qquad (2.\ 65)$$

with $Ia(n=2) = \frac{1}{32}$, $Ib(n=2) = \frac{3}{32}$ named respectively parallel and series noise.
Input preamplifier signal is a pulse with charge Qo therefore the input shaper signal is the same pulse amplified by Cin/Cf.

The output shaper maximum value is:

$$h(t=tm)\times Qo\frac{Cin}{Cf}=0.2306\times Qo\frac{Cin}{Cf} \qquad (2.\ 66)$$

If $\tau_{pa} << \tau_{ssh}$ (Table 2.12).

Thus from equation 2.59:

$$ENC(p.e.)=\frac{Qs\times Vn}{Vs}=\frac{Qo}{1.6\times10^{-19}C\times0.2306\times Qo\frac{Cin}{Cf}}\left(\frac{\sqrt{Ia(2)}\times enCtot}{Cf\sqrt{\tau}}\oplus\frac{\sqrt{Ib(2)}\times in\sqrt{\tau}}{Cf}\right)=$$

$$=\frac{1}{1.6\times10^{-19}C\times0.2306\times Cin}\left(\frac{\sqrt{Ia(2)}\times enCtot}{\sqrt{\tau}}\oplus\sqrt{Ib(2)}\times in\sqrt{\tau}\right)= \qquad (2.\ 67)$$

$$=\frac{1}{1.6\times10^{-19}C\times0.2306\times Cin}\left(\frac{\sqrt{Ia(2)}\times enCtot}{\sqrt{\tau}}\oplus\sqrt{Ib(2)}\times in\sqrt{\tau}\right)$$

From this formula derives that the series noise decrease with $\sqrt{\tau}$ and the parallel noise increase with $\sqrt{\tau}$.

The PARISROC slow shaper general schematic is represented in Figure 2.56: a typical two stage CRRC² filter with variable peaking time.
The peaking time can be set from 50 ns (default value) to 200 ns by the switched feedback capacitors.

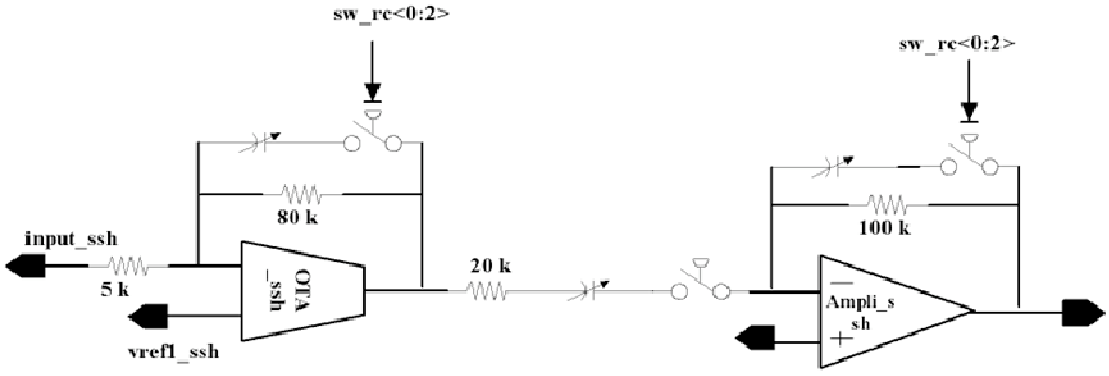

Figure 2.56. Slow shaper general schematic.

The Slow shaper output waveforms are illustrated in Figure 2.57 injecting an input signal of 1 p.e. and changing the shaping times (at a preamplifier gain of 8).
The slow shaper responses give 19 mV at tmax= 39 ns for the RC= 50 ns (green curve); 10 mV at tmax= 67 ns for RC= 100 ns (red curve) and 5 mV at tmax= 128 ns for RC= 200 ns (blue curve); showing that the maximum voltage value is inversely proportional to the shaping time.
The slow shaper output voltage DC level is 1 V.

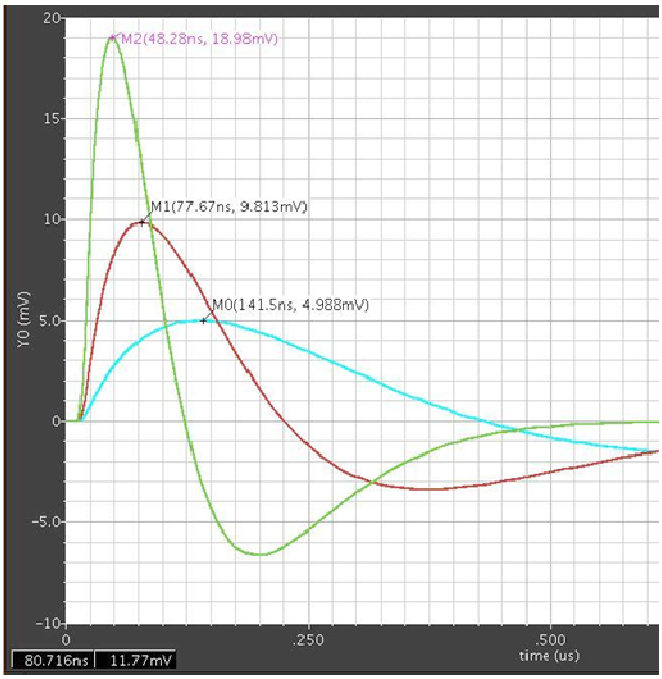

Figure 2.57. Simulated slow shaper output waveforms for an input signal of 1 pe and different shaping time: green curve for RC=50ns; red curve for RC=100ns and the blue curve for RC=200ns at a preamplifier gain of 8.

Now with τpa= 6 ns, are calculated the different λ:

$$\lambda_1 = \frac{\tau_{pa}}{\tau_1} = \frac{6ns}{50ns} = 0.12;$$

$$\lambda_2 = \frac{\tau_{pa}}{\tau_2} = \frac{6ns}{100ns} = 0.06;$$

$$\lambda_3 = \frac{\tau_{pa}}{\tau_3} = \frac{6ns}{200ns} = 0.03.$$

Looking at the Table 2.12 these λ values allow approximating the input shaper signal with a Dirac delta, even if, calculating the values:

$$\frac{t_{\max 1}}{\tau_1} = 0.816;$$

$$\frac{t_{\max 2}}{\tau_2} = 0.67;$$

$$\frac{t_{\max 3}}{\tau_3} = 0.64.$$

It is evident that increasing τ_{ssh}, the coefficient is getting to the theoretical value 0.56 τ for a Dirac at the input.
The slow shaper noise is simulated and represented in the following picture (Figure 2.58) that shown the rms noise values versus the frequency for the different shaping times; the values at 10 MHz are listed in the Table 2.13 at a preamplifier gain of 8.

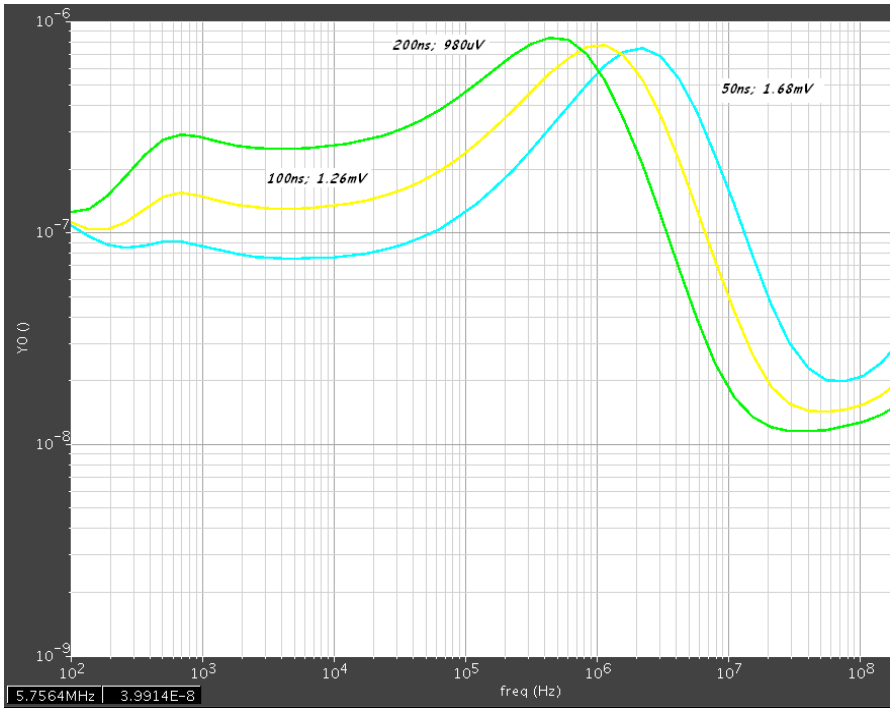

Figure 2.58. Simulated slow shaper rms noise values versus the frequency for the different shaping times: blue curve for RC= 50 ns; yellow curve for RC= 100 ns and the green curve for RC= 200 ns at a preamplifier gain of 8.

Gpa=8			
Time constant	**Vout (1pe)**	**Rms noise Slow Shaper**	**S/N**
50ns	19mV @ Tp=39ns	1.68mV ~1/11 pe ~ 14 fC	11
100ns	10mV @ Tp=67ns	1.2mV ~ 1/8 pe ~ 19 fC	8
200ns	5mV @ Tp= 128ns	0.980mV ~ 1/5 pe ~ 32 fC	5

Table 2.13. Simulated slow shaper rms noise values at 10 MHz for the different shaping times at a preamplifier gain of 8.

The shaper linearity performance is also simulated and plotted (Figure 2.59). The plot displays the maximum shaper output value versus the injected variable input charge (from 0 to 300 pe) and for different time constants.
Setting the preamplifier gain at 8, simulations indicate a good slow shaper linearity with residuals from -0.5 to 0.2 % at τ= 50 ns, from -1 to 0.3 % at 100 ns and -0.7 to 0.3 % at τ= 200 ns.
The dynamic range of the slow shaper is limited in comparison to preamplifier dynamic range because of the slow shaper saturation. This is not a real limit in terms of performance considering that a small dynamic range for high gain is enough.

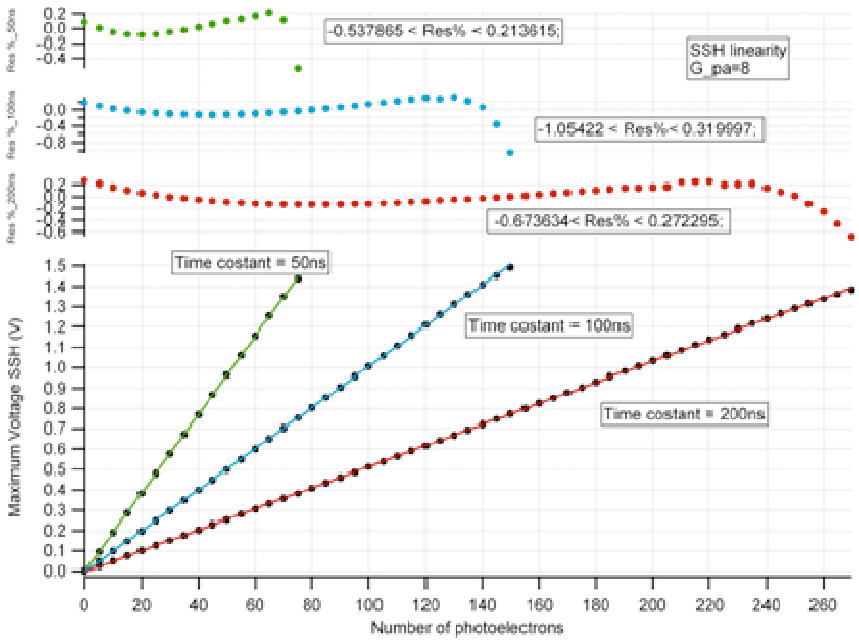

Figure 2.59. Simulated slow shaper linearity at a preamplifier gain of 8: green curve for RC= 50 ns; blue curve for RC= 100 ns and red curve for RC= 200 ns.

Gpa= 8			
Time constant	**Vout_max (V)**	**Qi_max©/npe**	**Residuals (%)**
50ns	1.437	12.8pC/80pe	-0.5 to 0.2%
100ns	1.493	24pC/150pe	-1 to 0.3%
200ns	1.385	48pC/300pe	-0.7to 0.3

Table 2.14. Slow shaper linearity results at a preamplifier gain of 8.

4.3. Fast channel

The PARISROC ASIC is a self-triggered device, meaning that the chip can be autonomous and decide when to convert charge and time. As such, it requires circuitry that senses whether a pulse exceeds a threshold: the fast channel has been designed for this purpose.
The amplified signal flows feeds two channels: the slow one (described previously) and the fast one.
The fast channel is made by a fast shaper followed by a discriminator. The fast shaper is a CRRC filter with a time constant of 15 ns. Its high gain allows to send big signal to the discriminator and thus to trigger easily on 1/3 of photoelectron. The noise affects not only the resolution of the amplitude measurement but it also determines the minimum detectable signal threshold. In fact, without input signal, the noise will be superimposed on the baseline and same fraction of the noise pulses will cross the discriminator threshold inducing a trigger (§ 6 Chapter III).
The fast shaper has a classical design (Figure 2.60): NPN differential pair to reduce the offset and for speed performance, followed by a buffer.

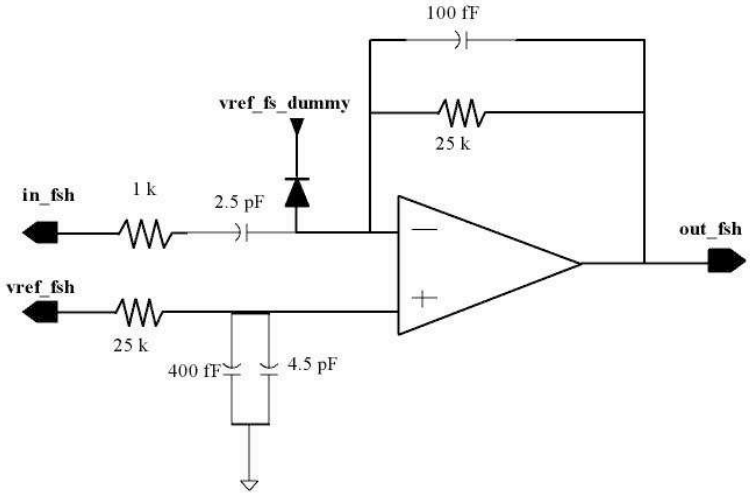

Figure 2.60. Fast shaper general schematics.

The purpose of this shaper is to filter the noise and to generate a high fast signal for time measurement. Figure 2.61 and Figure 2.62 represent the fast shaper output waveforms for a variable input signal. On the first figure are shown the waveforms injecting an input charge from 1 to 30 pe with step of 1 pe and on second from 1 to 2 pe with step of 0.1 pe. Table 2.15 lists the fast shaper principal characteristics obtained in simulation.

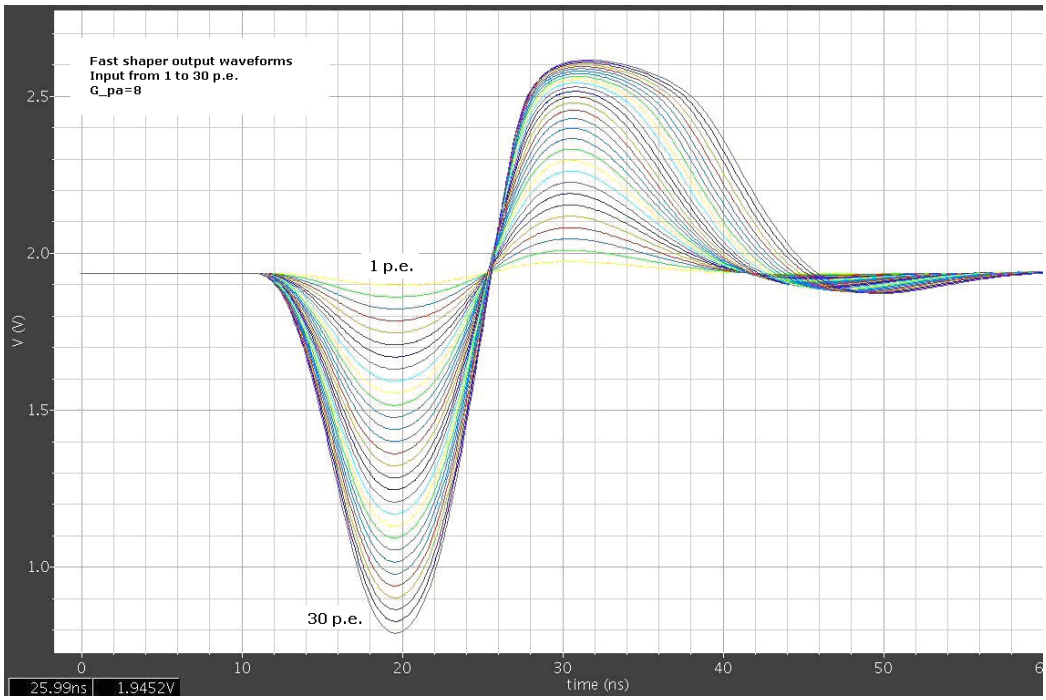

Figure 2.61. Simulated fast shaper outputs waveforms with input from 1 to 30pe; Gain (pa) = 8

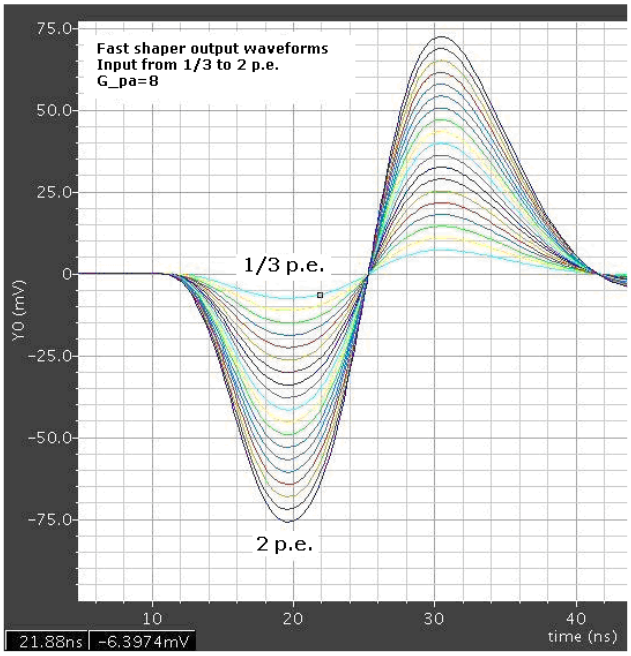

Figure 2.62. Simulated fast shaper outputs waveforms with inputs from 1/3 to 2 pe; Gain (pa) = 8.

Rms noise (V)	2.36 mV ~1/16 pe ~ 10 fC
SNR	16
Vout(1pe)(V)	39mV
Tp (1pe) (s)	8 ns

Table 2.15. Fast shaper simulated results. Gain (pa) = 8.

The fast shaper theoretical study gives an open loop gain of 57 dB (700); an f_{3dB} of 1.6 MHz and a cut-off frequency at 700 MHz. The simulation is illustrated in the following picture (Figure 2.63).

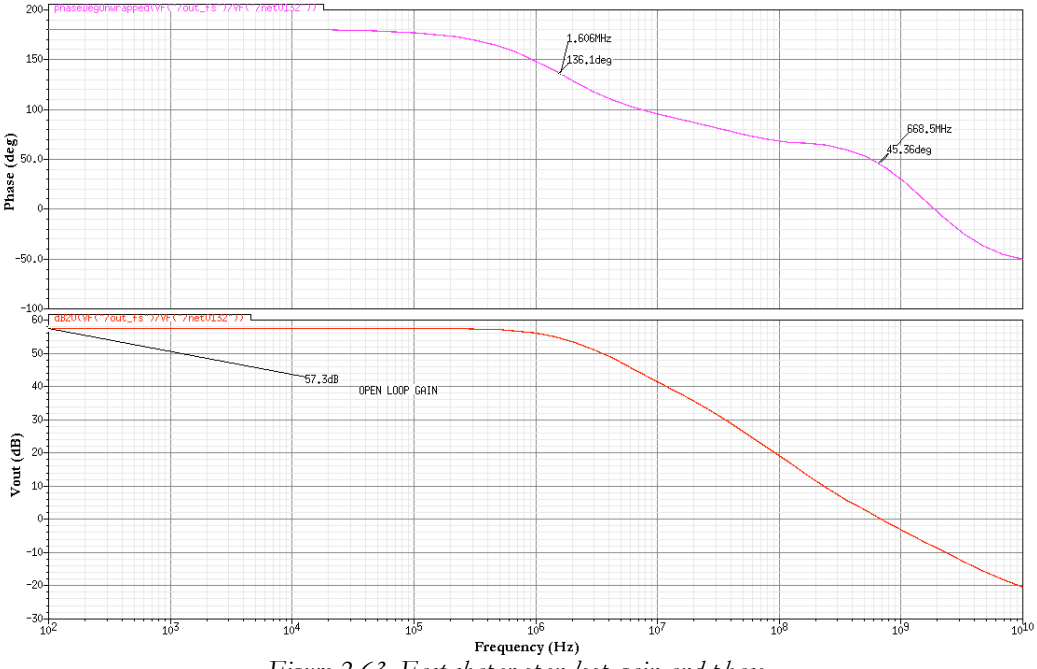

Figure 2.63. Fast shaper open loop gain and phase.

Figure 2.64 displays the beta factor of 34.42 dB and Figure 2.65 the loop gain and the phase of 104°.

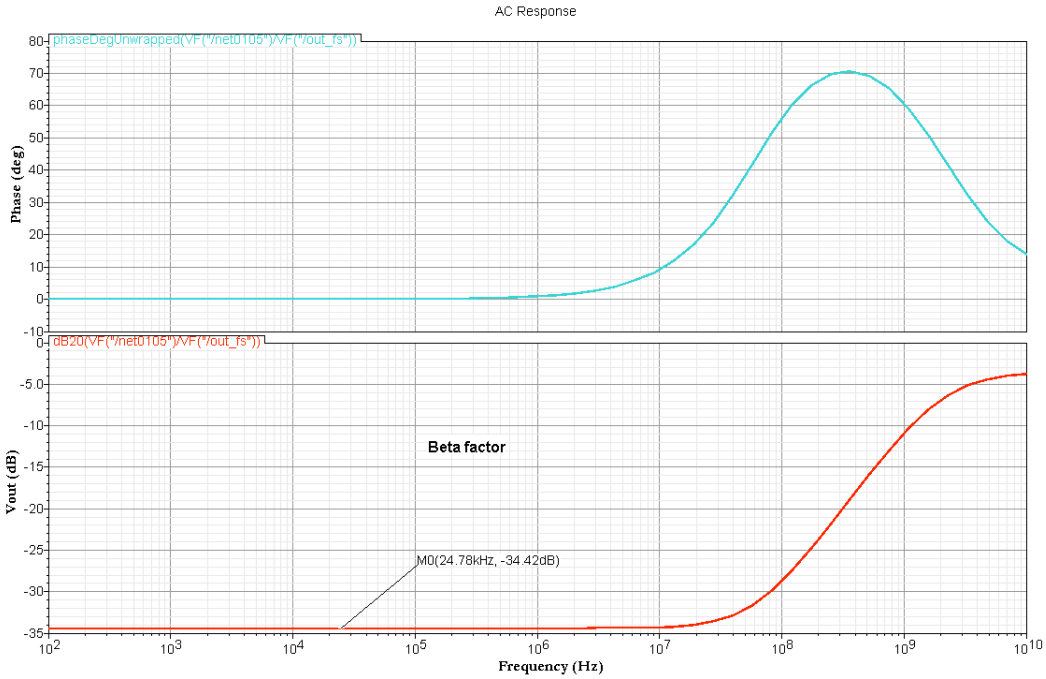

Figure 2.64. Fast shaper beta factor.

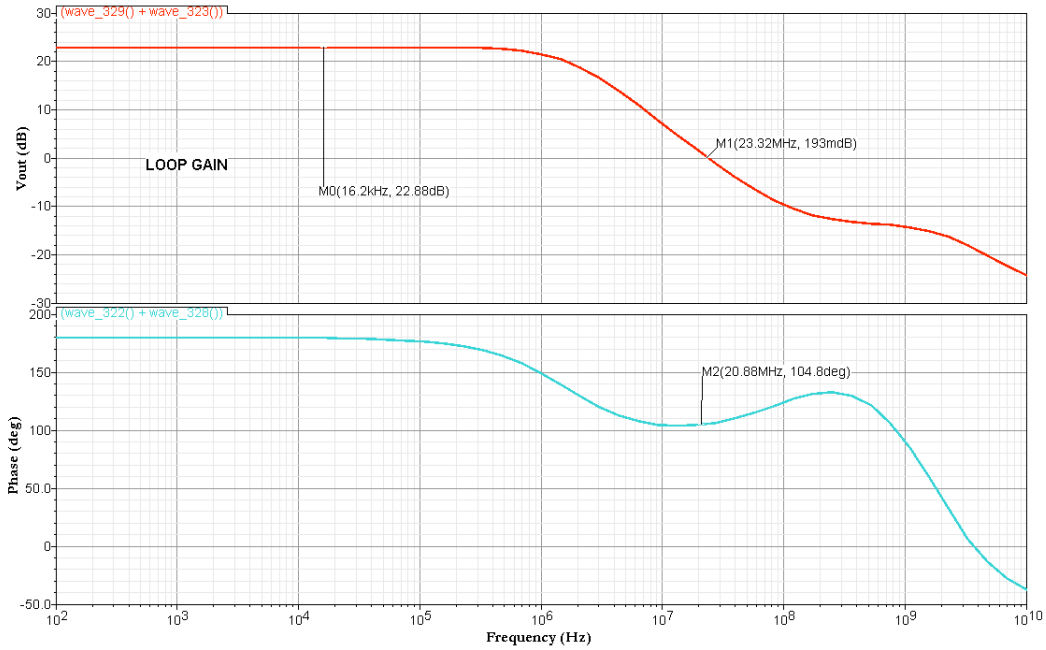

Figure 2.65. Fast shaper loop gain.

The fast shaper is followed by a low offset discriminator to trigger down to 50 fC (1/3 pe). As it is shown in Figure 2.66, the discriminator is really made by 2 discriminators; both of them can be used alone. Their outputs are multiplexed to ease the choice.

Both are simple low offset comparators with the same structure formed by a differential NPN pair with a resistive load to get a gain around 30, while insuring low offset. It is followed by a second PMOS differential pair. The performance is very good with an offset lower than 1 mV *rms* while maintaining high speed and low power consumption (100 µW).

The difference between the two discriminators comes from the way to set the threshold. The first discriminator has the threshold set by one 10-bit DAC, common to all 16 channels, and one 4-bit DAC for each channel. The second discriminator has the threshold set by only the 10 bit common DAC. Another difference is that the first discriminator is followed by a delay cell which calibrates and delays (Figure 2.67) the trigger until it holds the state of the response in SCA channel. The delay is variable with a minimum value of 25 ns in order to hold the charge signal at the maximum of slow shaper output signal (§ 4.4 Chapter II). A multiplexer in the discriminator output has been added to allow the use of an external trigger. Each trigger output can be disabled in case of necessity individually if desired.

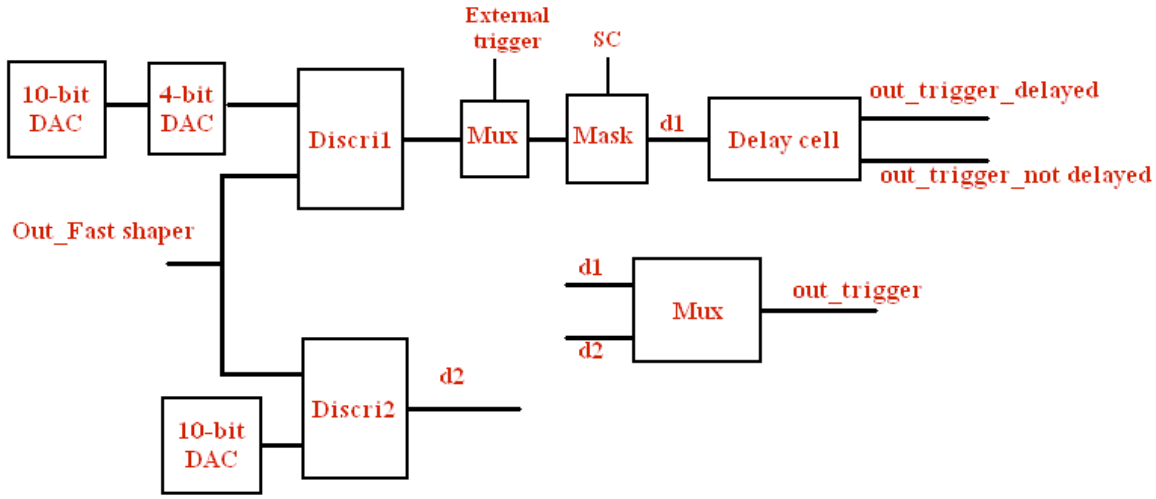

Figure 2.66. Discriminator cell schematic.

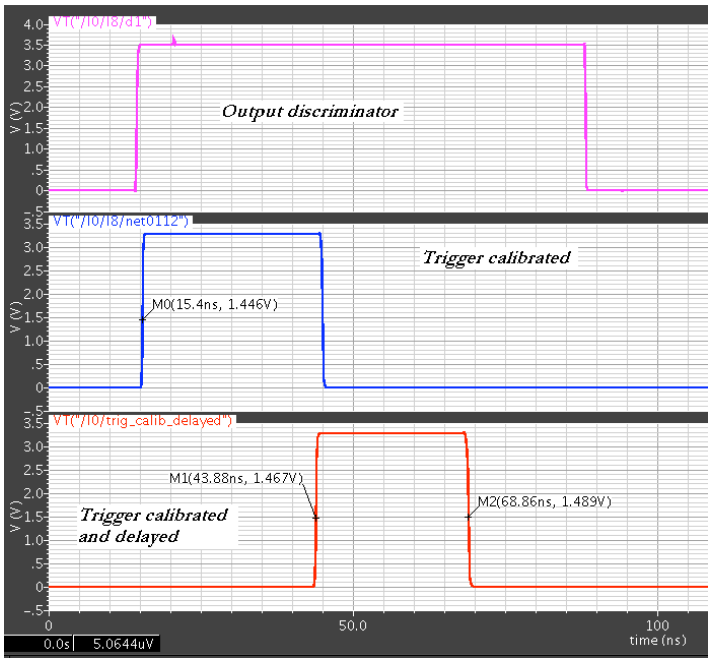

Figure 2.67. Simulated output trigger. Pink curve is the discriminator output trigger; the blue curve the calibrated trigger and the red curve the calibrated and delayed trigger.

The time at which the signal crosses a fixed threshold depends on pulse amplitude [23]. As the amplitude varies, the timing of the signal shifts, therefore variations in signal amplitude can spoil the timing distribution. This phenomenon is called "time walk".

On Figure 2.68 are displayed the output fast shaper waveforms and the trigger signals for a variable input charge (from 1/3 to 2 pe) and for preamplifier gain[43] of 14. On Figure 2.69 is displayed the zoom of the triggers rising edge in order to calculate the time walk of around 5 ns.
In order to reduce it, it is necessary to improve the fast shaper speed but this improvement will lead to increase the noise. It is known that the signal slope is proportional to the bandwidth whereas the rms noise is proportional to the square root of the bandwidth, so the choice is a compromise between noise and time walk performances.

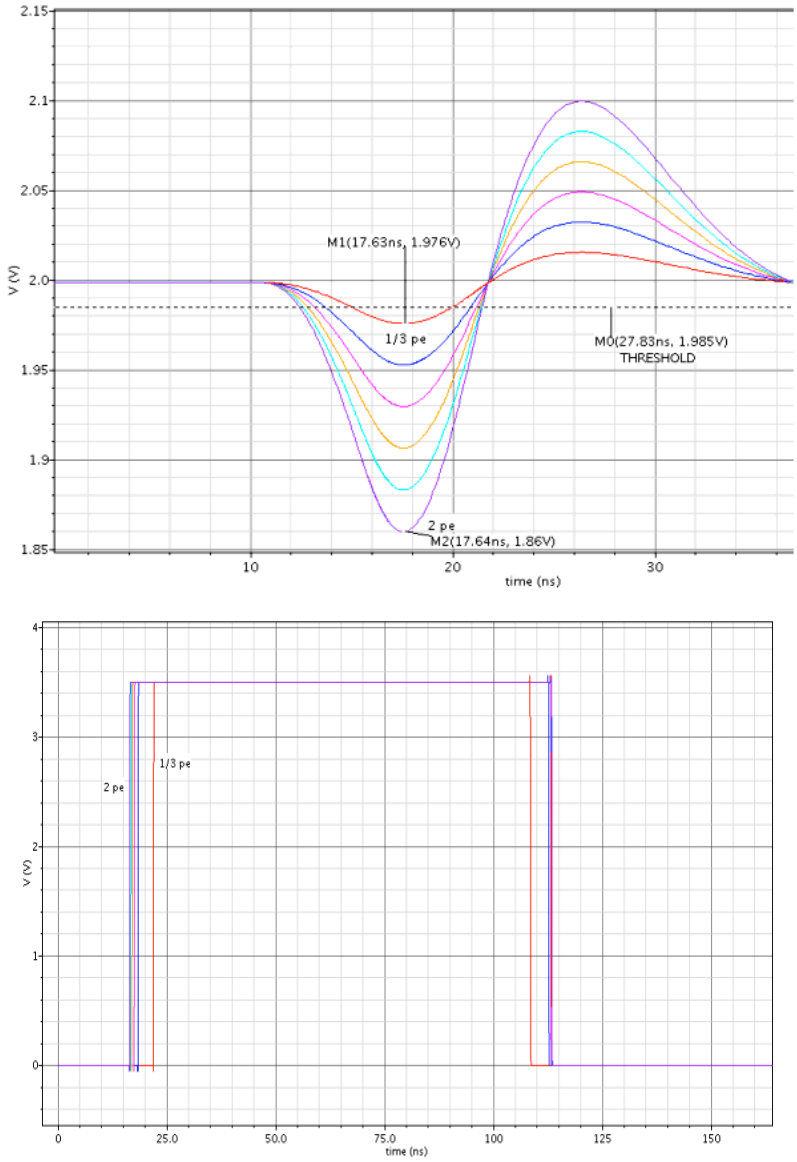

Figure 2.68. Simulated output fast shaper and trigger outputs (input charge from 1/3 to 2 p.e; threshold at 1/4 p.e ~ 15 mV at Gpa= 14).

[43] The choice of this preamplifier gain improves the simulations for small signals.

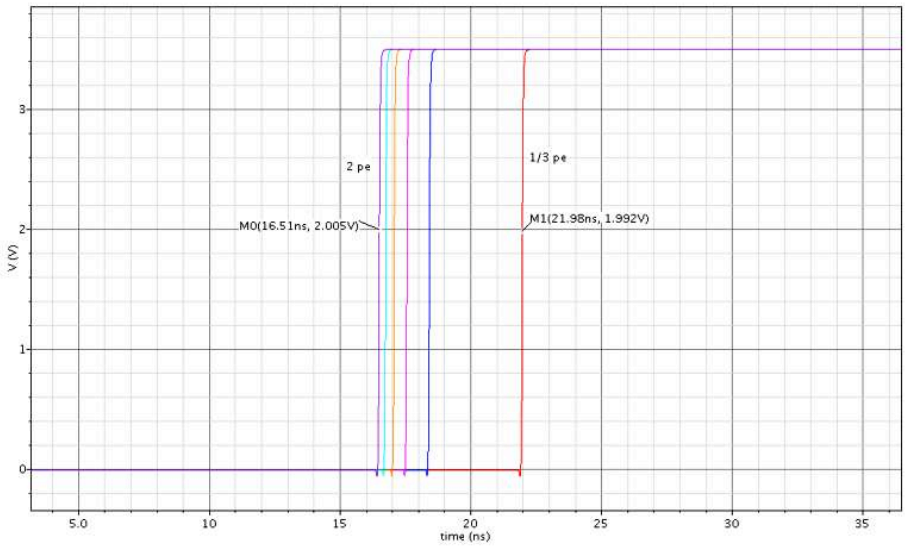

Figure 2.69. Zoom of triggers. Time walk ~ 5ns

As explained previously, two 10-bit DACs are used to set the discriminator threshold on the 16 channels, and a 4-bit DAC to improve the threshold setting on each channel. The 10-bit DAC architecture (Figure 2.70) is made from a variable current source (that supply a current named in the picture *Iref*) and an OTA. The variable current source is an array of 10 switched current sources driven by a common reference source.

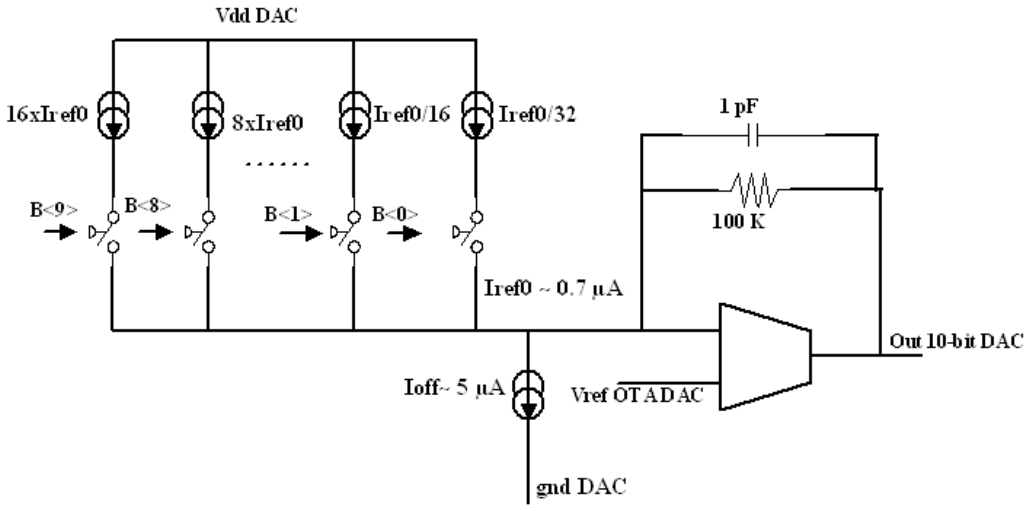

Figure 2.70. 10-bit DAC general schematic.

The currents Iref0 and Ioff0, indicated in Figure 2.70, can be changed by an external resistor and are used to adjust the dynamic range of the DAC.
The current that flows in the OTA feedback, named *Iota*, is given by:
Iota = Ioff - Ii, where *Ioff is* the current supply by another current source that can be considered as a default value.
$Iota_{max} = Ii_{min}$ gives the maximum value of the DAC output voltage (named *Vout 10-bit DAC*), whereas $Iota_{min} = Ii_{max}$ gives the minimum value of the DAC output voltage,
Therefore the DAC output voltage is given by *Vout 10-bit DAC= Vref_dac + 100 kΩ * Iota.*
With Vref_dac= 2 V the minimum and maximum voltages obtained in simulation are:

Vmin= 167 mV and Vmax= 2.34 V then the minimum voltage step value (named LSB[44]) has value given by:

$$LSB = \frac{V\max - V\min}{2^n} = 2.12mV \qquad (2.\ 68)$$

With a fast shaper response of 39 mV for 1 p.e. in its input, the discriminator threshold can be set with a step of 1/18 of pe common to all the channels.

The 4-bit DAC added for each channel is made from the voltage reference of the 10-bit DAC and 4 switched current source (Figure 2.71)

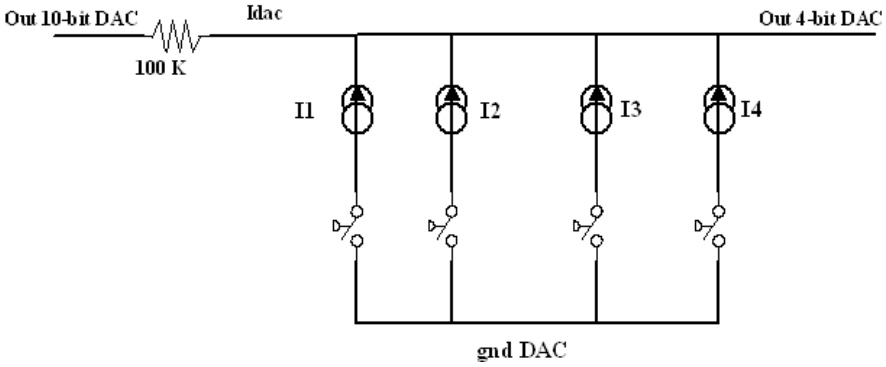

Figure 2.71. 4-bit DAC general schematic.

With $I_2 = 2I_1$; $I_3 = 4I_1$; $I_4 = 8I_1$.

The 4-bit DAC output voltage (named *Vout 4-bit DAC*) is obtained by: *Vout 4-bit DAC = Vout 10-bit DAC – Rdac* * Idac where *Rdac* is the resistance indicated on figure 2.72 of 100 kΩ and *Idac* the total current supply by the current source on Figure 2.71 given by the sum of the single current *Ii* (with i=1 to 4).

The minimum voltage step value for this 4-bit DAC is given by:

$$LSB = \frac{V\max - V\min}{2^n} = 60mV \qquad (2.\ 69)$$

Where:

- *Vmax= Vout_dac_10 bit s* - Rdac * Imin is given by the minimum current injected;
- *Vmin= Vout_dac_10 bit s* - Rdac * Imax by the maximum current.

The 4-bit DAC has been designed to set the threshold precisely in each channel but with an LSB of 60mV this is not achievable. This DAC will not be used in the measurements explained in Chapter III but by an external resistor its bias current and then the Idac can be changed to reduce the LSB value.

4.4. SCA Channel

The SCA[45] channel is made of two parts:

- A digital part to create the Track and Hold (T&H) signal and to control the management of the two T&H cells;
- The two T&H cells to each time and charge measurements.

[44] Least Significant Bit.

[45] A dual Track and Hold.

The SCA has a depth of two; this means that there are two capacitors to store the values for each T&H cell: for time measurement as well as for charge measurement (Figure 2.72).

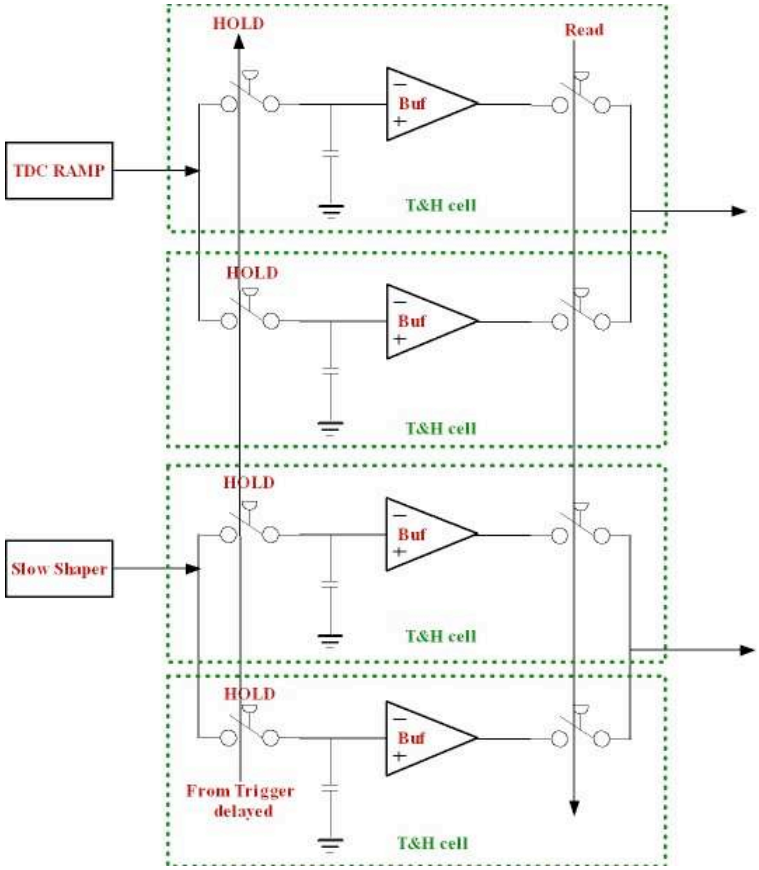

Figure 2.72. SCA (switched capacitor array) general scheme.

On Figure 2.73 is illustrated the T&H cell mode of operation: an output trigger signal is produced and sent to the SCA cell. This trigger is calibrated and delayed in the discriminator cell and is used to create the Track and Hold signal that closes the "Hold switch" (Figure 2.72) to memorize the charge and time values in the T&H capacitor (500 fF).

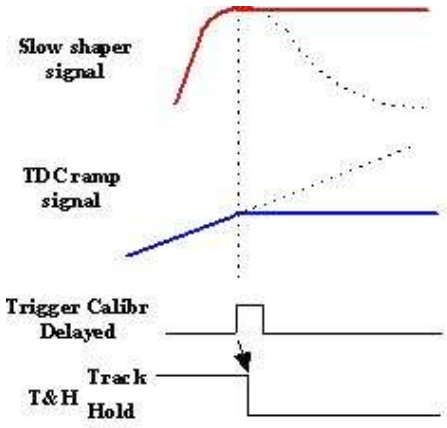

Figure 2.73. T&H cell mode of operation.

The T&H signal allows to save the content of the capacitor value only when a trigger occurs and when the selected column (read signal) is sent by the digital part to close the "Read switch" (Figure 2.74)
The SCA column is selected, read and erased by the digital part.

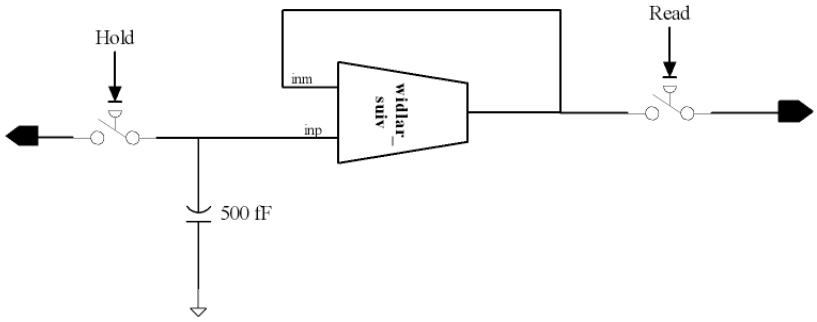

Figure 2.74. One T&H cell general schematic.

On Figure 2.75 the charge SCA simulation is shown. The hold signal (green curve) that closes the "Hold switch" exactly at the maximum value of the slow shaper signal (red curve). This voltage value is memorized in the capacitor and read when the "read signal" (violet curve) closes the "Read switch". The voltage signal (yellow curve), that brought the charge information, is now at the output of the SCA cell, available to be converted by the Analog to Digital Converter (ADC) in a digital value.
The conception of a trigger calibrated and delayed depends on the necessity to hold the maximum slow shaper value: the trigger signal must be delayed according to the shaping time that is variable.

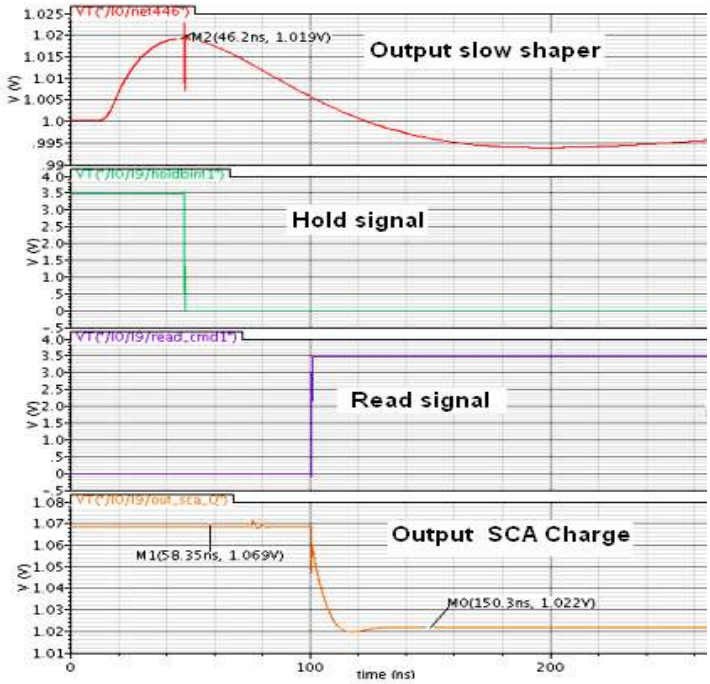

Figure 2.75. Slow shaper and SCA simulation. The Slow shaper maximum value (first picture) is then memorized in the SCA (bottom picture) as DC level thanks to the delayed trigger that switch off the T&H (second picture).

At the same time, for time measurement, the TDC ramp (§ 4.5 Chapter II), is sent in the T&H time cell, as done for the charge measurement, the calibrated and delayed signal closes the "Hold switch" at the in the two T&H cells. The TDC ramp voltage value is memorized in the capacitor and read when the "Read switched" is closed.

The time voltage value is converted then by the ADC. Figure 2.76 illustrates the SCA time simulation: when the T&H switch is closed by the T&H signal (green curve) the TDC voltage level (red curve) is saved in the capacitor and read (violet curve) in the output of SCA (yellow curve).

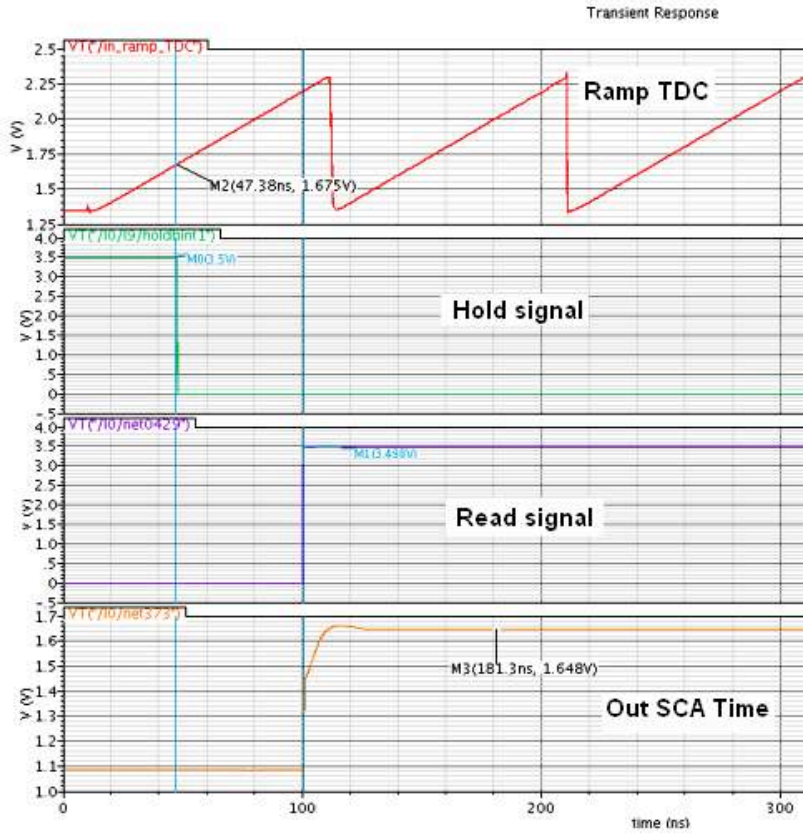

Figure 2.76. TDC ramp and SCA simulation. The TDC voltage value (first picture) is then memorized in the SCA (bottom picture) as DC level thanks to the delayed trigger that switch off the T&H (second picture).

4.5. Time measurements

The time measurement is a crucial point of the ASIC that allows the measurement of a "coarse time" and a "fine time".

The "coarse time" (Timestamp) is performed by a 24-bit Gray Counter located inside the digital part. The coarse time resolution is of 100 ns (clock of 10 MHz) and the counter overflows each 1.67 s [21].
As shown in Figure 2.77, this time is then saved in a 24-bit register when the T&H signal indicates the detected signal. A start signal launches the counter and an external reset is provided to synchronize all the PMm² chips inside the experiment.

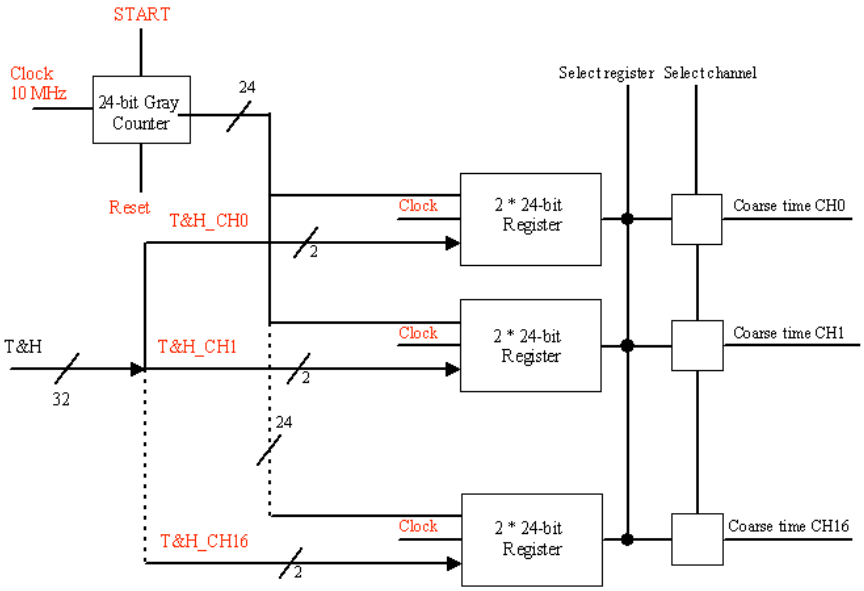

Figure 2.77. Timestamp general schematic.

The fine time measurement is performed by the SCA (§ 4.4 Chapter II) which samples a 12-bit TDC ramp (100 ns), common for all channels, at the same time of the charge.

TDC ramp cell (see Figure 2.78) is composed of two main parts: analog part and digital part. The analog part includes the current source generator and integrator while the digital part contains a delay cell and some logic which controls the charging and discharging of the capacitor. In Figure 2.78 is represented the TDC Ramp general schematic.
The ramp generator is formed by the reference current generator and an integrator. The reference current flows into the amplifier input and is integrated in the feedback capacitor. The current, which flows in feedback, charges the capacitance Cf when the switch is off and when the switch is turned on, Cf discharges so the output of the amplifier gets a ramp voltage wave.
A Signal, named "start ramp", sent by the digital part and synchronized with the 10 MHz clock (clock of the timestamp), manages the switch. The rising signal starts the ramp and the falling signal stop the ramp (Figure 2.79). The start ramp signal is delayed until being sent in the TDC ramp cell.

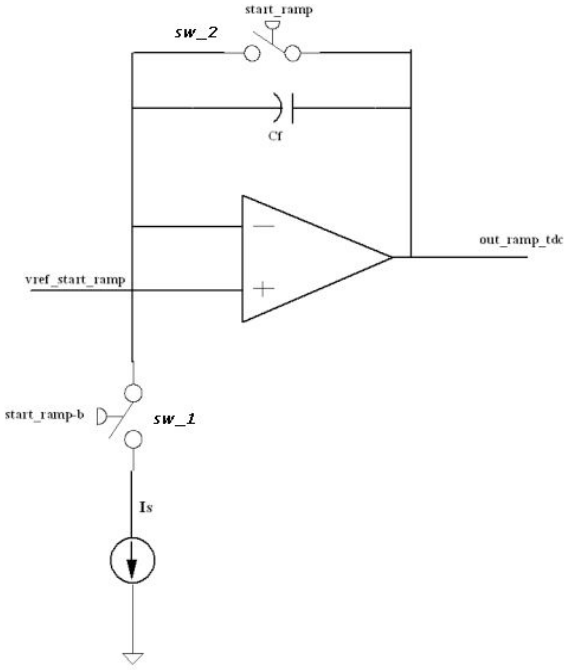

Figure 2.78. TDC ramp general schematic.

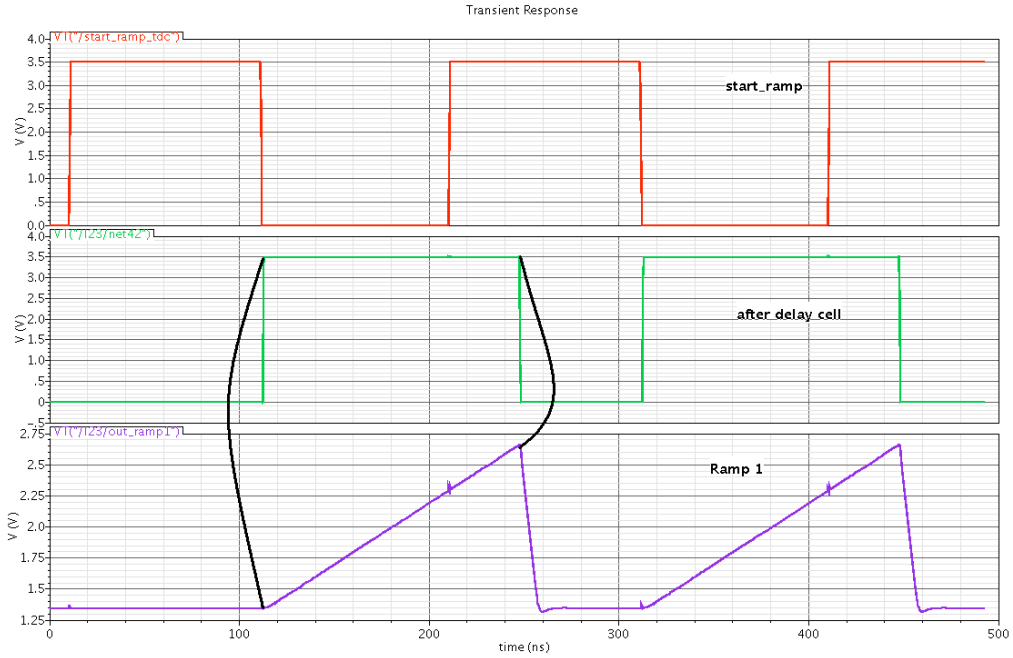

Figure 2.79. The TDC ramp simulation with start ramp signal and start ramp signal delayed that creates the ramp.

The conception of a self-triggered device with a random signal imposes time measurement in the full time field and with a minimum dead time.

For this reason the real ramp is created from two ramps (Figure 2.83). This structure avoids the large falling time (Figure 2.80) and therefore the recovery time of the ramp (that creates a dead zone for time measurements) due to the Cf discharge time. In this way, when one ramp is stopped and needs to be recovered, another ramp is ready for work.

Other problems are: the glitch in the start of the ramp due to the switching on of the feedback switch and a non linearity in the end of the ramp. In Figure 2.80 the problems of non linearity and the recovery time of the ramp are emphasized.

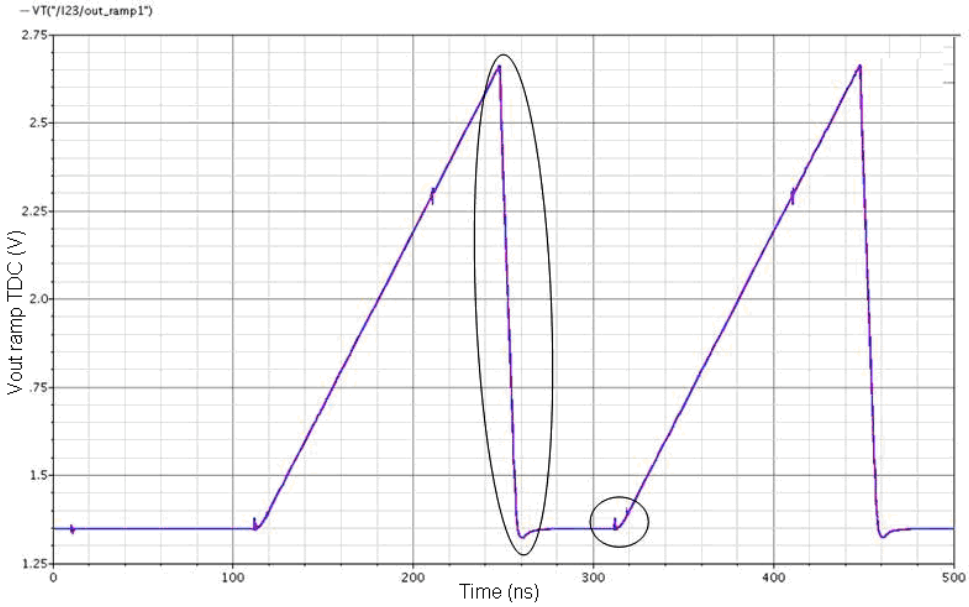

Figure 2.80. TDC ramp. Problems of not linearity are emphasized on the beginning and on the end of the ramp.

In Figure 2.81 the TDC cell structure is represented: the signal start ramp, coming from the digital part, enters in two delay cells. For one of the two ramps this signal is inverted before. The two delayed signals create the first and second ramps. Commutating alternatively two switches, the 100 ns ramp TDC is created.
In such way the two ramp generators are working in parallel in different period.

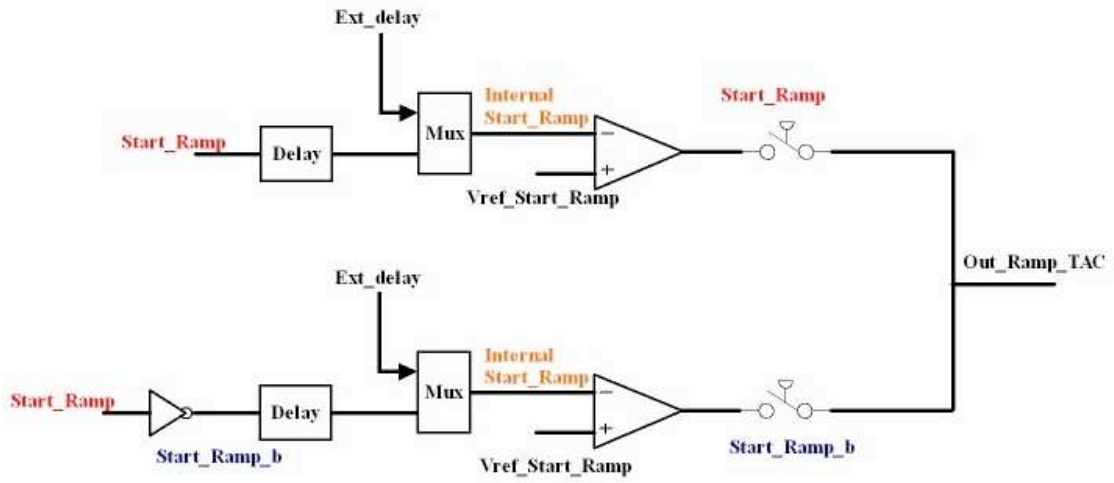

Figure 2.81. TDC Ramp scheme.

Figure 2.82 illustrates that for the first ramp, the delayed start ramp signal starts and stops the integration and for the second ramp the start ramp signal is inverted and then delayed to start and stop the integration of the ramp.

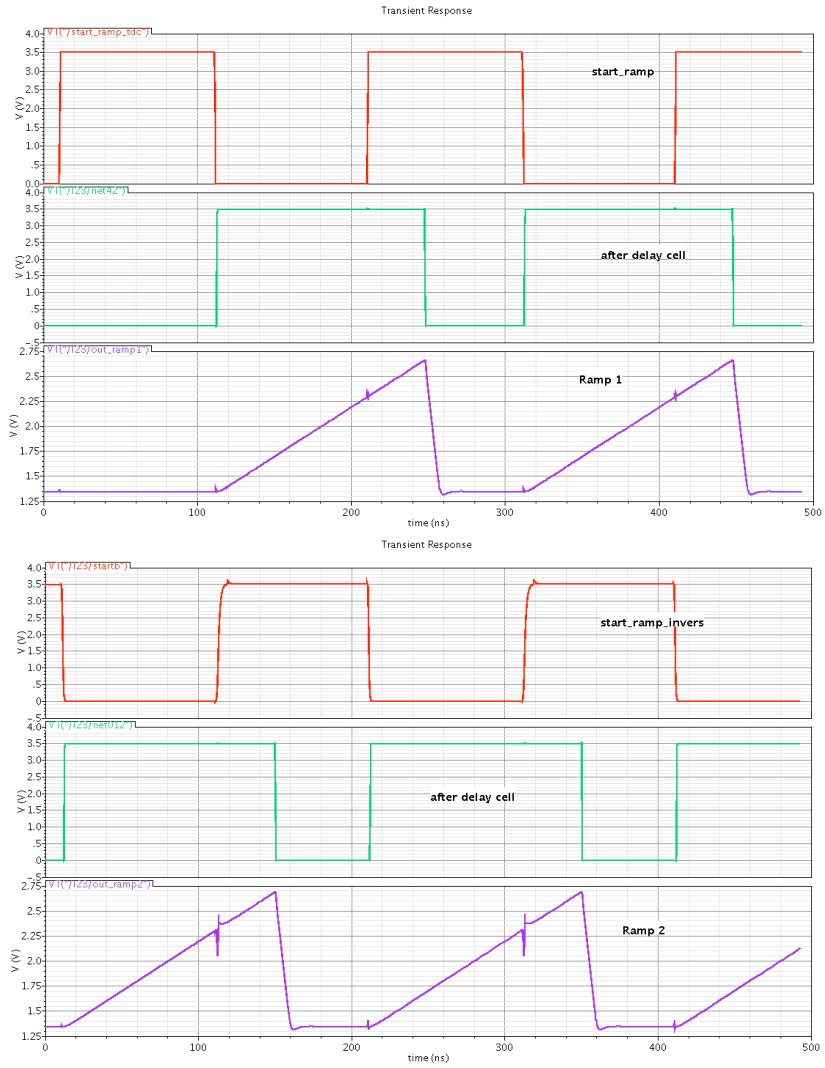

Figure 2.82. TDC Ramp simulations. On the top the TDC ramp one with red signal: start ramp, green signal: start ramp delayed; on the bottom the TDC ramp 2 with red signal: start ramp inverted, green signal: start ramp inverted and delayed.

Moreover the solution for the non-linear region at the beginning and ending time of the ramp wave is the choice of a little longer working time (~130 ns) than 100 ns for the two ramps. This allows to use the ramps in the linear region: looking at the Figure 2.83, in which are shown the simulated signals as the start ramp signal on the top of the picture, the TDC ramp 1, TDC ramp 2 and the total ramp on the bottom, it is evident that the edge of start ramp clock starts the ramp, but the control signal for the end of each ramp is generated by a delay cell from start ramp clock with a fixed delay.
From this graph it is clear that at any edge of start ramp clock, though one of the ramps is in non-linear region, the other ramp keeps running in linear region. As a result, linear region covers the entire time field.

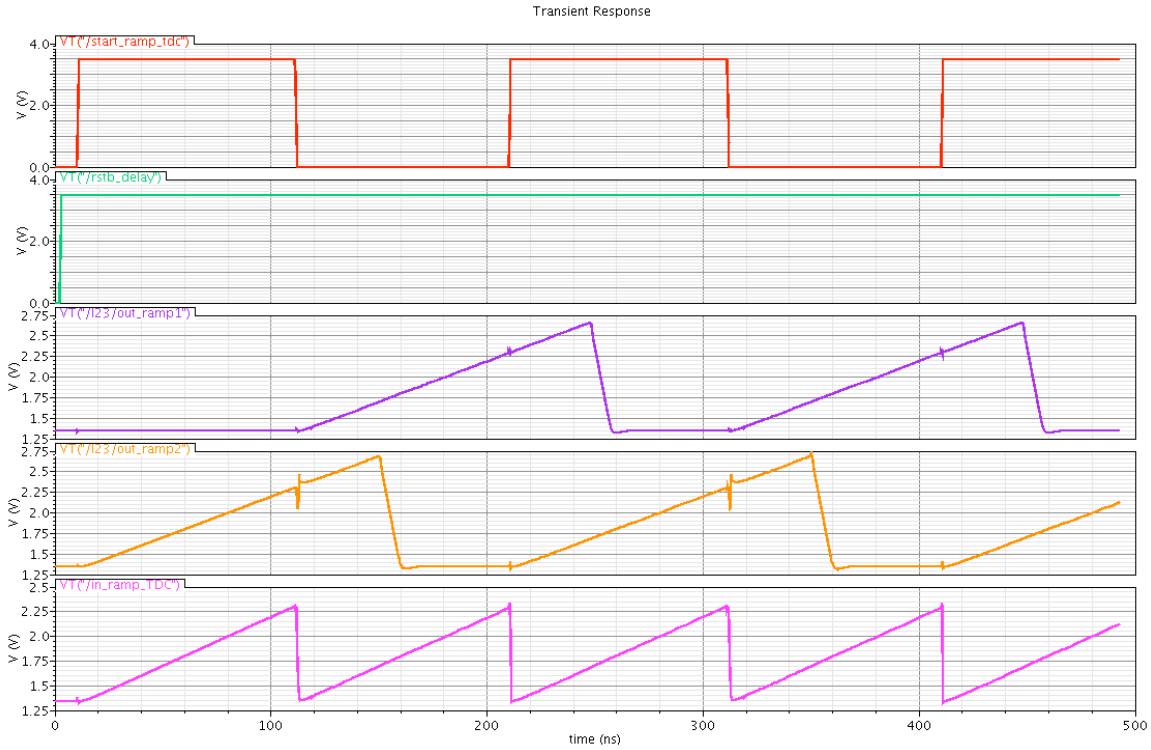

Figure 2.83. TDC ramp simulation. Start ramp signal on the top of the picture; TDC ramp 1, TDC ramp 2 and the total ramp on the bottom.

The total ramp is sent to the T&H time cell. So the load of the TDC ramp is made of 32 track-and-hold capacitors in total. With this consideration, the value of the track and hold capacitance is 0.5 pF for each channel, so finally the load capacitor is of 16 pF.
The T&H generator has been designed to be suitable for the speed and load requirement.

4.6. Wilkinson ADC

For data storage and subsequent analysis the analog signals must be digitized. An internal Wilkinson ADC is implemented to convert the analog signals:

- The charge value;
- The time value.

Signals are stored in the SCA and then converted in digital values by a 16 channel common ADC Ramp. Figure 2.84 illustrates the general schematic: a discriminator with a ramp as reference, common for charge and time values in each channel, is used to compare and to convert the data.

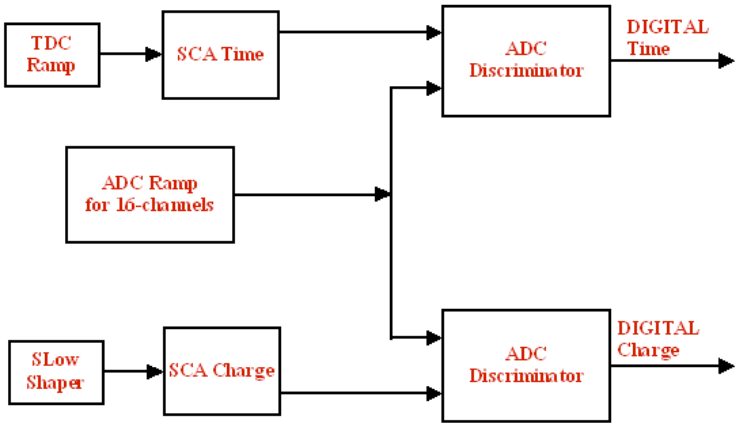

Figure 2.84. ADC general schematic.

When one or more channel are hit, the T&H signal indicates to the digital part that the SCA cell is full and so, after a fixed time of 200 ns the hit channels are loaded and the conversion is started. The "start ramp ADC" signal is sent to the ADC ramp cell and the 40 MHz counter (12-bit Gray Counter) is started. When the charge and the time of all the 16 channels are converted (32 conversions in 1 run) the digital part stops the conversion and then starts the readout of the data (Figure 2.85).

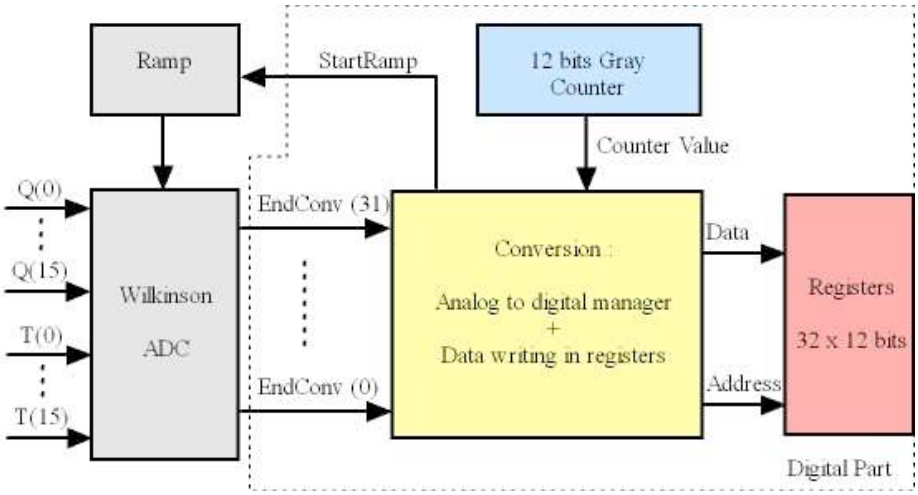

Figure 2.85. Conversion module.

In Figure 2.86 is represented the ramp ADC general scheme. It is the same as TDC ramp one, the difference comes from a variable current source which allows obtaining 8bit, 10bit and 12bit ADC according to the injected current.

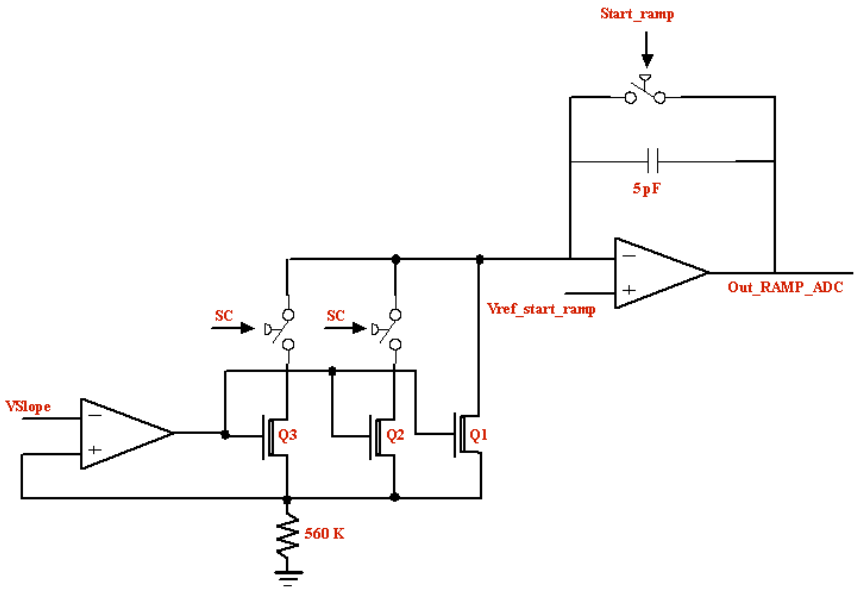

Figure 2.86. ADC ramp schematic.

The current source is made by an amplifier with a reference voltage named Vslope (0.564 V), that fixes the slope of the ADC ramp, and switches transistor (Q1, Q2 and Q3) with different dimensions:

- $\left(\frac{W}{L}\right)_3 = \frac{10\mu m}{10\mu m}$, that gives *I3=1.84 μA;*
- $\left(\frac{W}{L}\right)_2 = \frac{30\mu m}{10\mu m}$, that gives *I2=380 nA* and
- $\left(\frac{W}{L}\right)_1 = \frac{150\mu m}{10\mu m}$, that gives *I1=123 nA.*

The Vslope, given by the bandgap, fixes the voltage on the resistor (560 kΩ) and so the current.
The default value is 12-bit ADC when the two switches are open and the current is given by the transistor Q1. Closing the switch of Q2 the current I2 is added to I1 setting the 10-bit ADC ramp; equally closing the switch of Q3 (with Q2 switch open) the current I3 is added to I1 setting the 8-bit ADC ramp. In Figure 2.87 are shown the three ADC ramps.

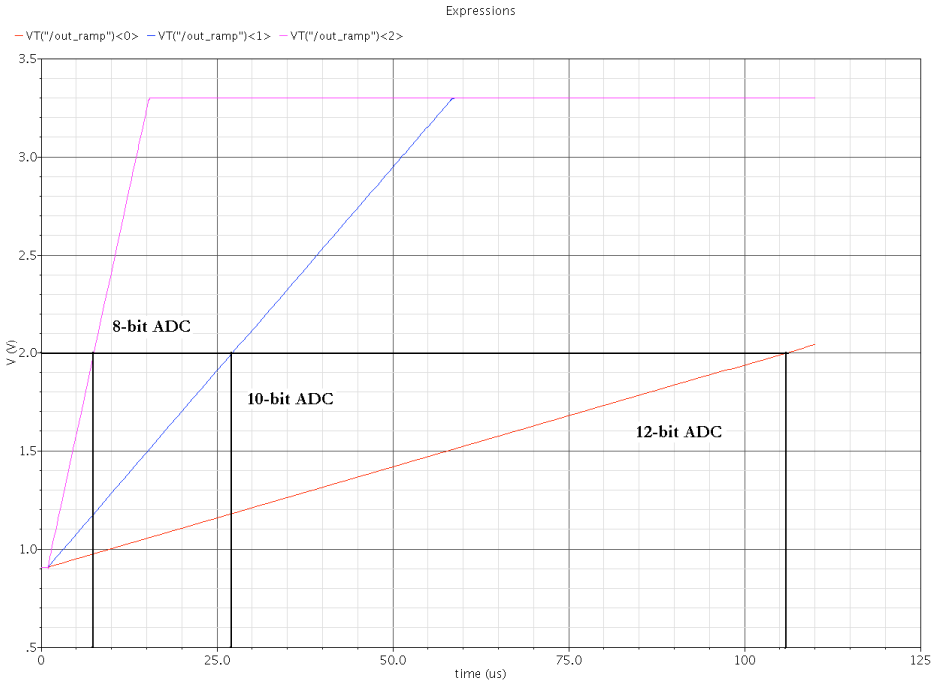

Figure 2.87. Simulated 8, 10, 12 ADC ramps.

The current produced by the current source is integrated in the feedback capacitor (Cf= 5 pF), with a reference voltage given by the bandgap (Vref start ramp= 0.907 V). The rising edge of the signal "start ramp ADC" (sent by the digital part) starts the integration, opening the feedback switch, up to 3.3 V. Closing the switch the feedback capacitor is discharged in order to allow a new integration. The switch is closed by the falling edge of the signal "start ramp ADC".
With a clock at 40 MHz the 12-bit ADC has a ramp of around 103 µs (2^{12} * 25 ns), the 10-bit ADC one of 25.6 µs (2^{10} * 25 ns) and the 8-bit ADC one of 6.4 µs (2^{8} * 25 ns).
Therefore, as illustrated in the Figure 2.87 the 12-bit ADC ramp starts at 0.9 V but stops at 2 V in 103 µs. A dynamic range of 1 V can be converted in digital values. Equally for the other ramps, the ramps stop at 3.3 V, but the 10-bit ADC ramp reaches 2 V at 25 µs and the 8-bit ramp s reaches 2V at 6.4 µ.
For the three ramps the dynamic range of conversion is from 0.9V to 2V.
Table 2.16 gives, for each ramp, the time duration to reach the maximum value, 2V.

12 bit ADC	From 0.9 V to 2 V in 102 µs LSB=260 µV
10 bit ADC	From 0.9 V to 2 V in 25.6 µs LSB=1.2 mV
8 bit ADC	From 0.9 V to 2 V in 6.4 µs LSB=3.8 mV

Table 2.16. ADC characteristics.

5. Conclusions

The long phase of theoretical study has led to the ASIC characterization. All the analog blocks have been simulated in terms of noise, output waveforms and linearity. Good results have been expected except that the noise dependence by the switched preamplifier input capacitance.
The ASIC performances have been tested in measurement as explained in the next chapter.

Chapter III

PARISROC Measurements

1. Introduction

The first version of PARISROC chip has been sent for fabrication in June 2008 to the AMS foundry (AustriaMicroSystems) through the CMP (Multi Project Center); a batch of 6 packaged ASICs and 20 dies have been produced and received in December 2008.
The cost of this fabrication is 17000 euro for 25 dies delivered. For prototype fabrication the price is a function of the surface of the dies; the total surface for the dies is about 19 mm² with a cost of 890 euro/mm².
For mass production the costs decrease to about 25 Euros per chip for 5000 chips and to 10 Euros per chip (packaging including) for 10000 chips.
Having received the ASIC a long phase of characterization has been started; this phase of measurements is important to verify the chip performance and to confirm its expected requirements. The comparison with the theoretical study allows the investigation.
In the design phase a series of implementations have been foreseen to facilitate the tests:

- Probes to observe the internal ASIC points;
- An extra ASIC input, common for all the channels;
- An external ADC input;
- An external trigger input.

2. ASIC Laboratory test

The PARISROC characterisation test has been a critical step in the project planning due to the ASIC complexity.
A test bench has been set up in the laboratory (Figure 3.1) to characterize the chip performance.
It involves essentially:

- A dedicated test board, described in the following section;
- A DC supply sets at +6.5 V and -8V;
- A signal generator to inject an input signal;
- An oscilloscope to visualize the analog output signals;
- A PC to manage the entire test bench;

A dedicated Labview[46] program sends the ASIC configuration (slow control parameters; ASIC parameters, etc) and receives the output bits via a USB cable connected to the test board. The test program and the test board are developed by the LAL "Tests group".

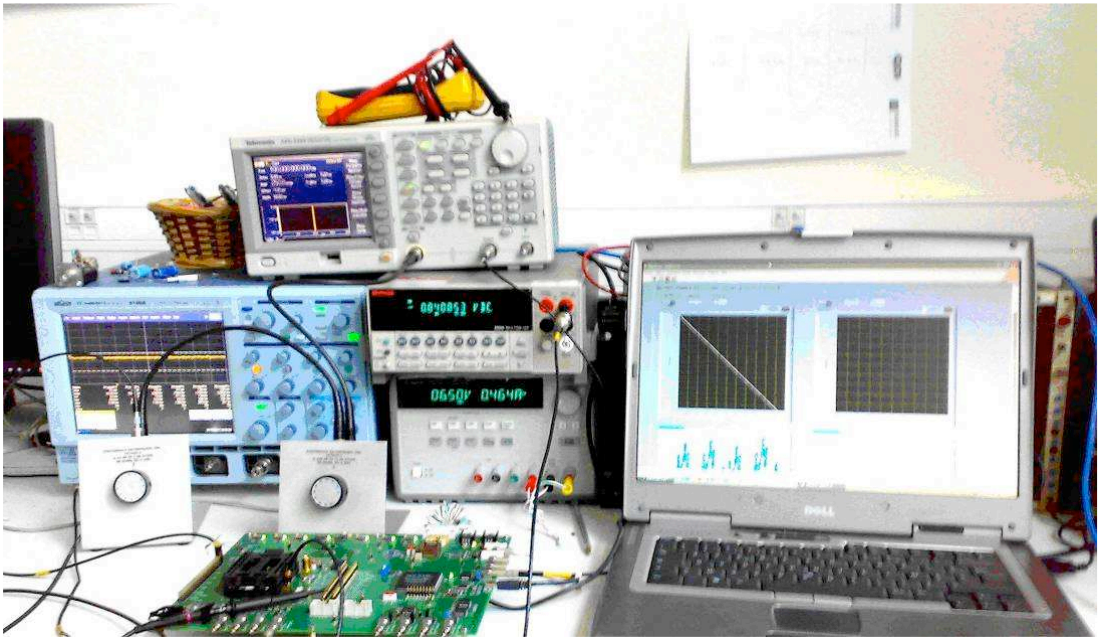

Figure 3.1. Test bench used in PARISROC ASIC measurements.

2.1. Test Board

A dedicated test board was designed and realized (Figure 3.2) to allow the characterization of the chip.

[46] Short for "Laboratory Virtual Instrumentation Engineering Workbench".

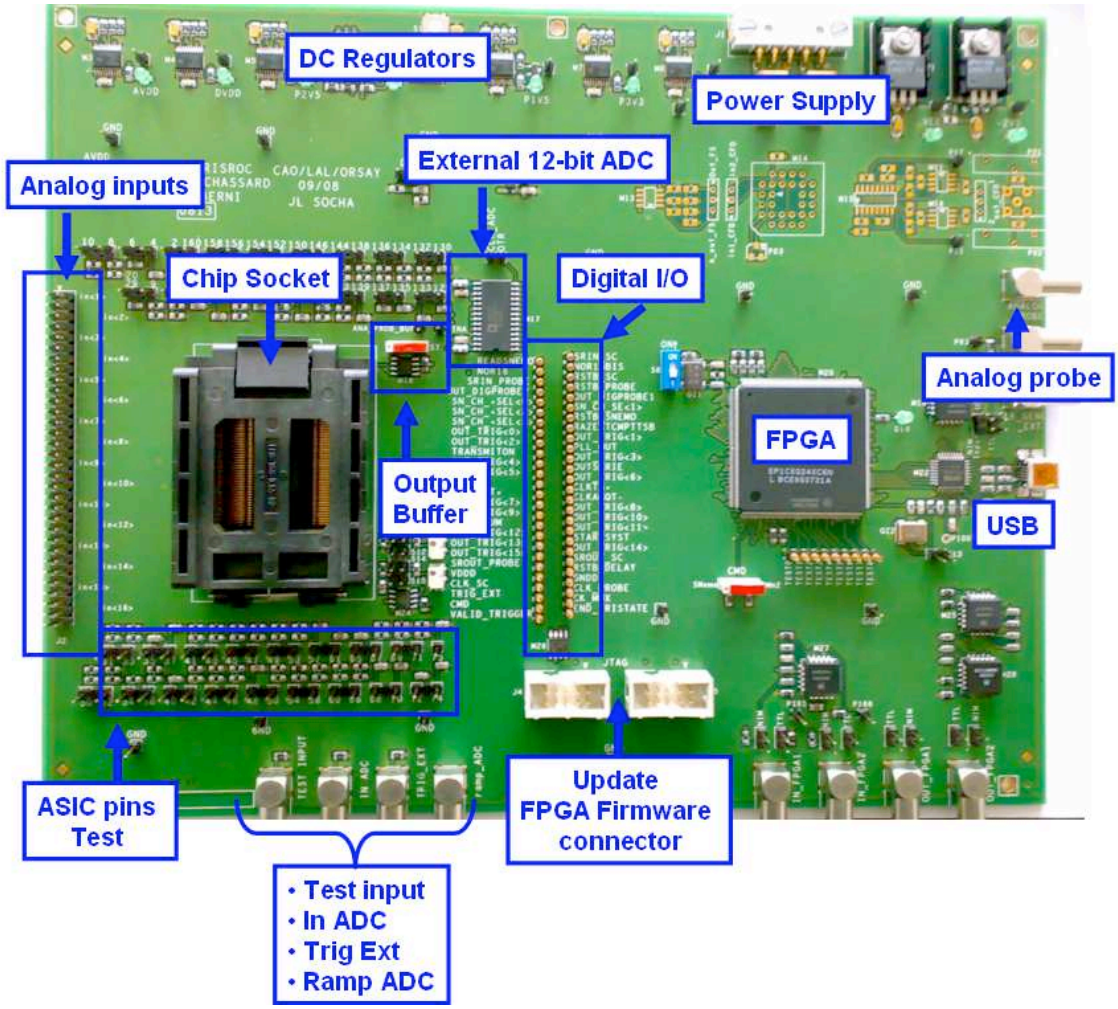

Figure 3.2. Test board.

The test board involves a socket to host the ASIC under test and a FPGA. This supplies all the slow control parameters and the two LVDS clocks and receives the digital output signals from the chip. The main part of the firmware inside the FPGA is written in VHDL[47] language and one part of this firmware makes the communication between the ASIC and the PC via a USB connection. The firmware can be updated via a JTAG interface. The communication between the PC and the board is managed by Labview program.

A 64-pin straight connector (16 inputs + 48 gnd) achieves the connection between the input signal and the 16 ASIC inputs.

The power supply of the test board is made from the DC supply by 7 different voltages regulators:

- Three 3.3 V to supply the ASIC and FPGA;
- A 2.5 V for LVDS signals;
- A 1.5 V for FPGA core;
- A ± 5 V to supply the output buffers.

Various test pins are placed to observe the digital signals and all the ASIC points. Specific input Lemo connectors are added to inject:

- Internal input test;
- Signal directly in the ADC input;
- External trigger;
- External ADC Ramp.

[47] Verilog Hardware description language.

An output Lemo connector named "Analog probe" is placed to observe the analog signals on the oscilloscope.
Each digital output can be driven with NIM or TTL levels which are the most standard logic levels.
An external ADC has been added on the test board to allow a second measurement path.

2.2. Dedicated Labview program

A dedicated Labview program has been developed to communicate with the ASIC test, it is structured in 6 tabs: *slow control* parameters tab, *words probe* choice, *DAC linearity* test, *Read ADC*, *ADC linearity* and *S-Curves* tests.
The data of each Labview tests are saved in a excel type file allowing easy performances analysis and statistical studies.
Figure 3.3 shows the "Slow control tab". The Slow control parameters (Annex I) are sent to change the ASIC configuration:

- The preamplifier parameters for the choice of input and feedback capacitors (to set the preamplifier gain) ;
- The DAC parameters to set the threshold of the two 10-bit DAC and the 4-bit DAC;
- The Discriminator mask to disable the output trigger for the selected channels;
- The DAC delay to chose the delay necessary to hold the slow shaper signal in its maximum value;
- The ADC precision choice (12,10 or 8-bitADC);
- The slow shaper shaping time (50,100,200 ns);
- Other bits to select particular functionalities.

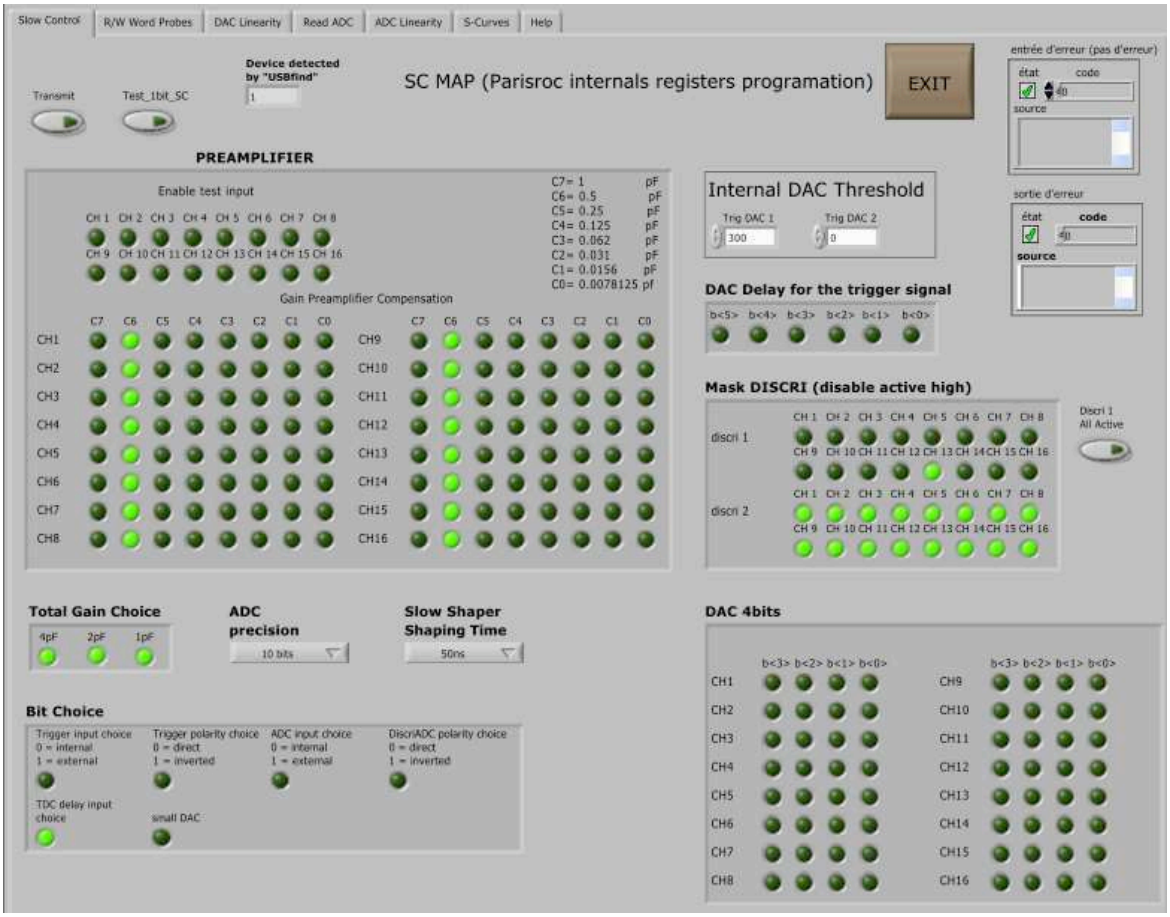

Figure 3.3. Labview Slow control tab.

Figure 3.4 shows "The words probe tab" composed by two elements the words section (in the top) and the probe section (in the bottom).
The words are register inside the FPGA that allows to drive the input pin of the ASIC and to manage internal module of the FPGA.
The probe section allows the choice of the different analog and digital signals to test with the oscilloscope:

- The analog probe allow to select the preamplifier, slow shaper, fast shaper and TDC ramp output signals and the choice of the channel in which the measurements will be done.
- The digital probe allow to select the Track and Hold, the start ramp ADC and TDC, the trigger signal delayed or not delayed.

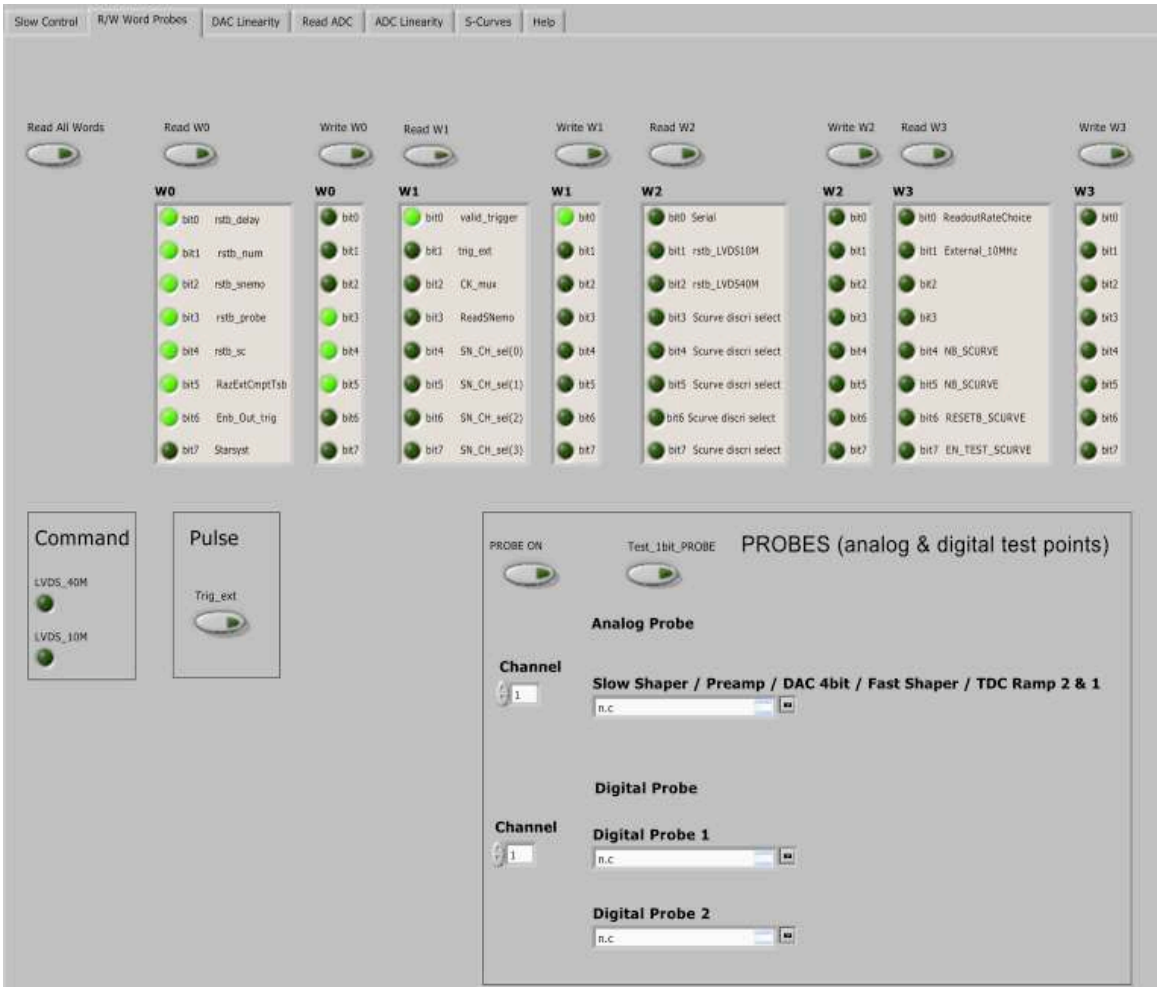

Figure 3.4. Labview words probe tab.

The third tab is conceived for "DAC linearity" measurements. As shown in Figure 3.5 the linearity of the two 10-bit DAC is plotted directly on the tab with its residuals. This gives a first idea of DAC performance until data study (§ 5 Chapter III).

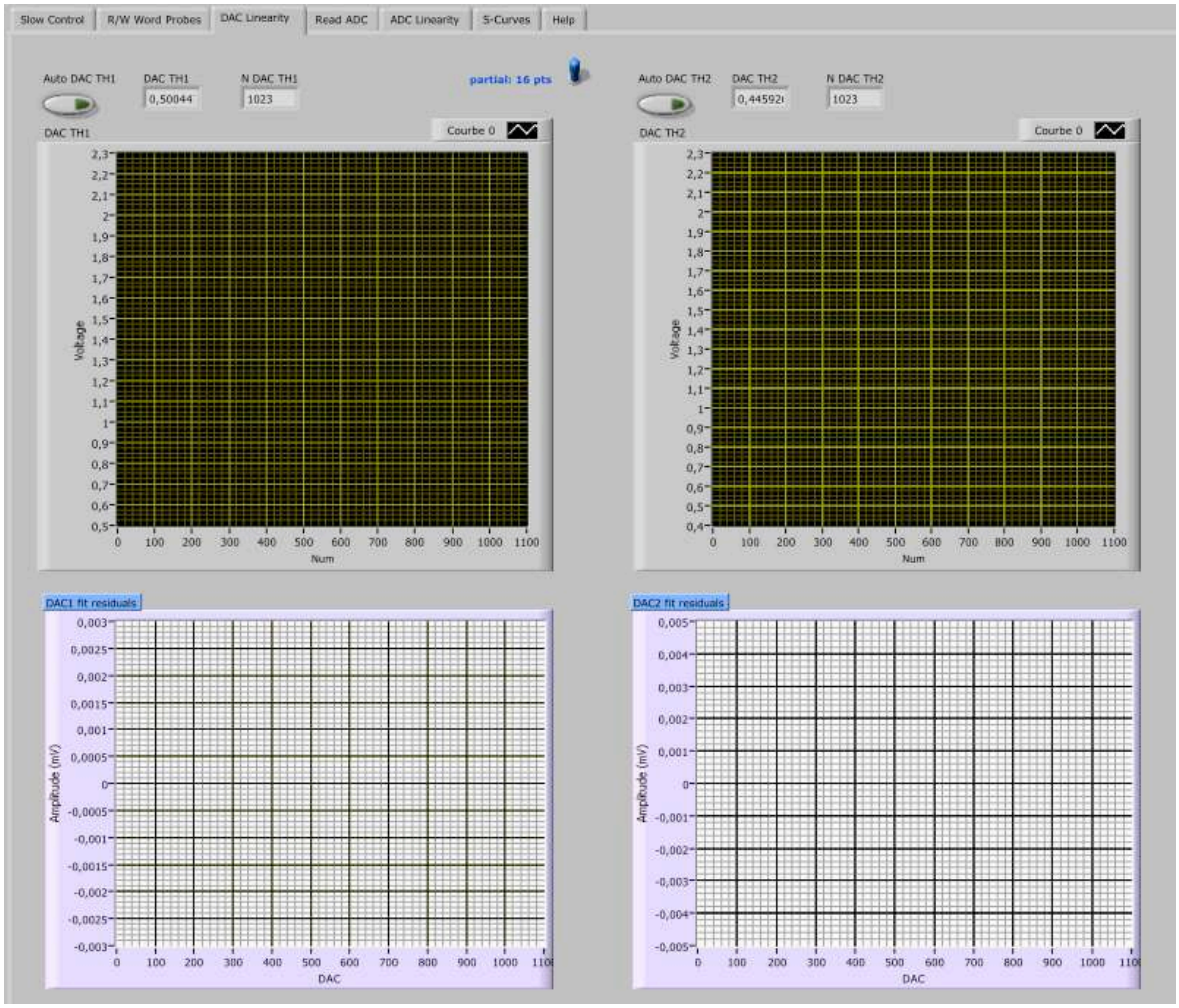

Figure 3.5. Labview DAC linearity tab.

Two tabs are dedicated to the ADC analysis:

- The first to charge measurements;
- The second to the ADC linearity.

The first tab is shown on Figure 3.6 and it is divided in two part; one to check the ADC performances injecting an external voltage and the second to test the whole chain injecting a signal in the input of the ASIC.
The first part works with an external trigger, made by the FPGA, and shows:

- The channel number, the time stamp, the fine time and the charge data for the 16 channels for one acquisition (on the top of the tab);
- The maximum, minimum and mean charge values as a function of the channel number (first plot on the bottom in the left side);
- The rms charge value for each channel (second plot on the bottom in the left side);
- The charge distribution for a single selected channel (third plot on the bottom in the left side).

The second part works with an internal trigger and displays the one channel charge distribution with its mean value, the standard deviation and the number of read events.

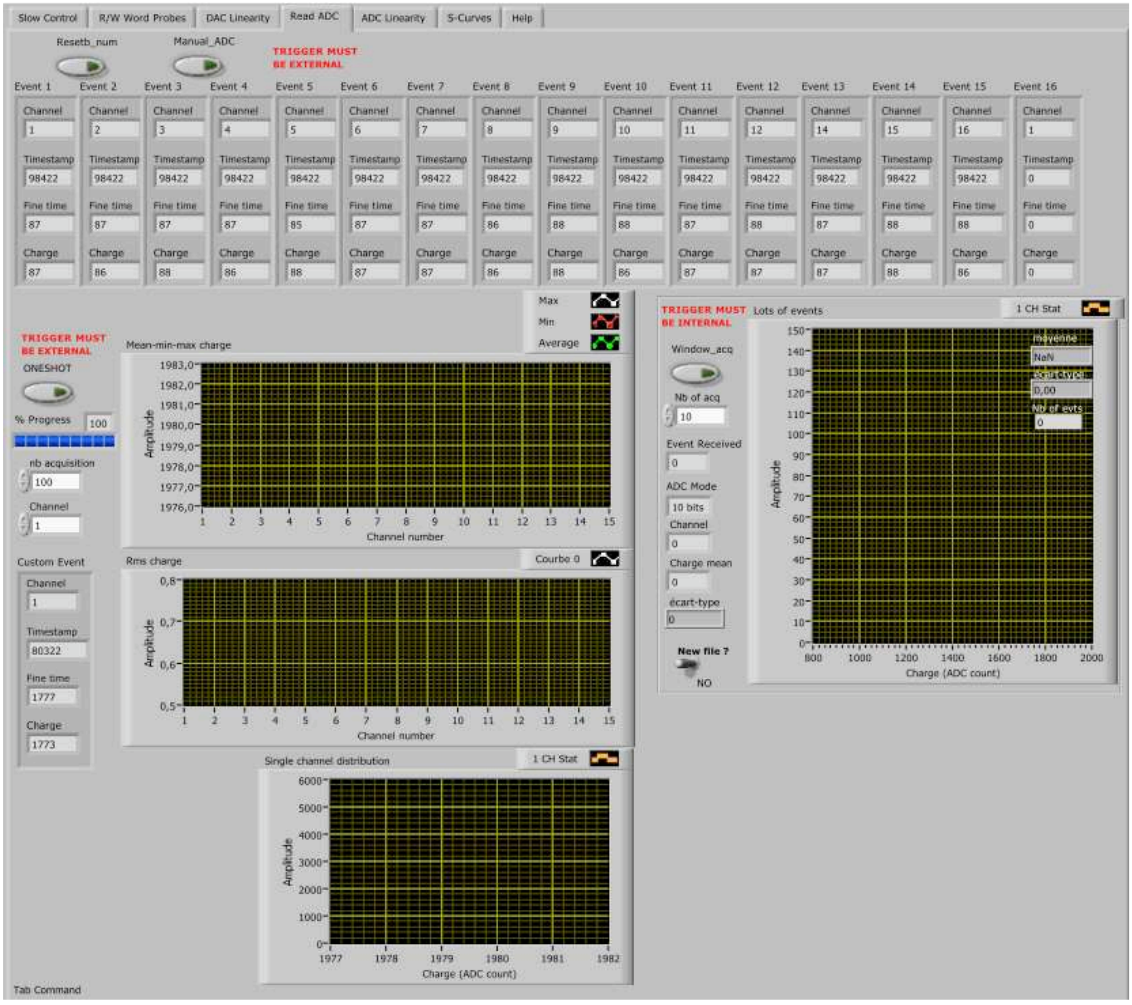

Figure 3.6. Labview Read ADC tab.

The second tab, shown in Figure 3.7, checks the ADC linearity performances injecting a variable external voltage in the ADC.
The ADC linearity can be tested in the left panel using a voltage signal given by the internal 10-bit DAC and the setting parameters are:

1. The number of bits of the ramp ADC;
2. The input signal dynamic range obtained setting the minimum and maximum DAC code;
3. The dimension of the input signal step variation (in LSB);
4. The channel number.

In the right panel with a voltage signal given by the power supply and the parameters involved are:

1. The power supply step dimension;
2. The number of the steps.

The ADC linearity and the residuals are plotted in the two sides of the tab. These give a first idea of the ADC performances. An accurate study has been done with these data, as explained in the following paragraphs (§ 7 Chapter III).

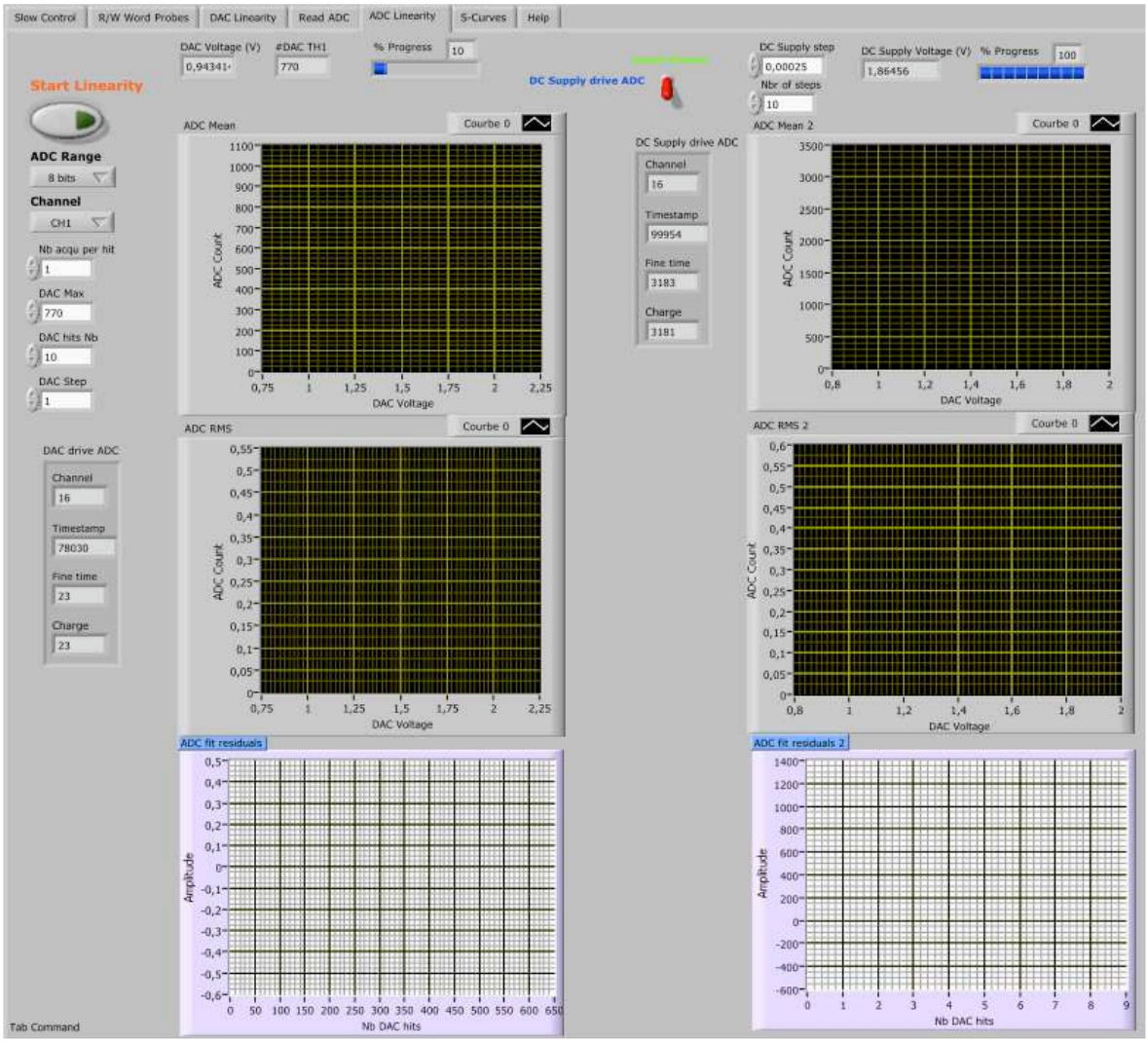

Figure 3.7. Labview ADC linearity tab.

The last tab (Figure 3.8) is dedicated to the S-Curve measurement explained in § 6.2 Chapter III.
The top portion of the panel allows the S-Curve test for each channel plotting the trigger efficiency in % versus the threshold level in DAC units.
The bottom portion allows the test of the 16 channels, one after the other, and displays:

- On the left side each S-Curve during its measurement;
- On the right side the 16 plots together at the end of the measurement.

The parameters involved in this section are:

- The choice of the discriminator (one or two);
- The channel number (from 1 to 16);
- The threshold dynamic range (setting the minimum et maximum value of the DAC and the step width);
- The number of the injected pulses then its frequency.

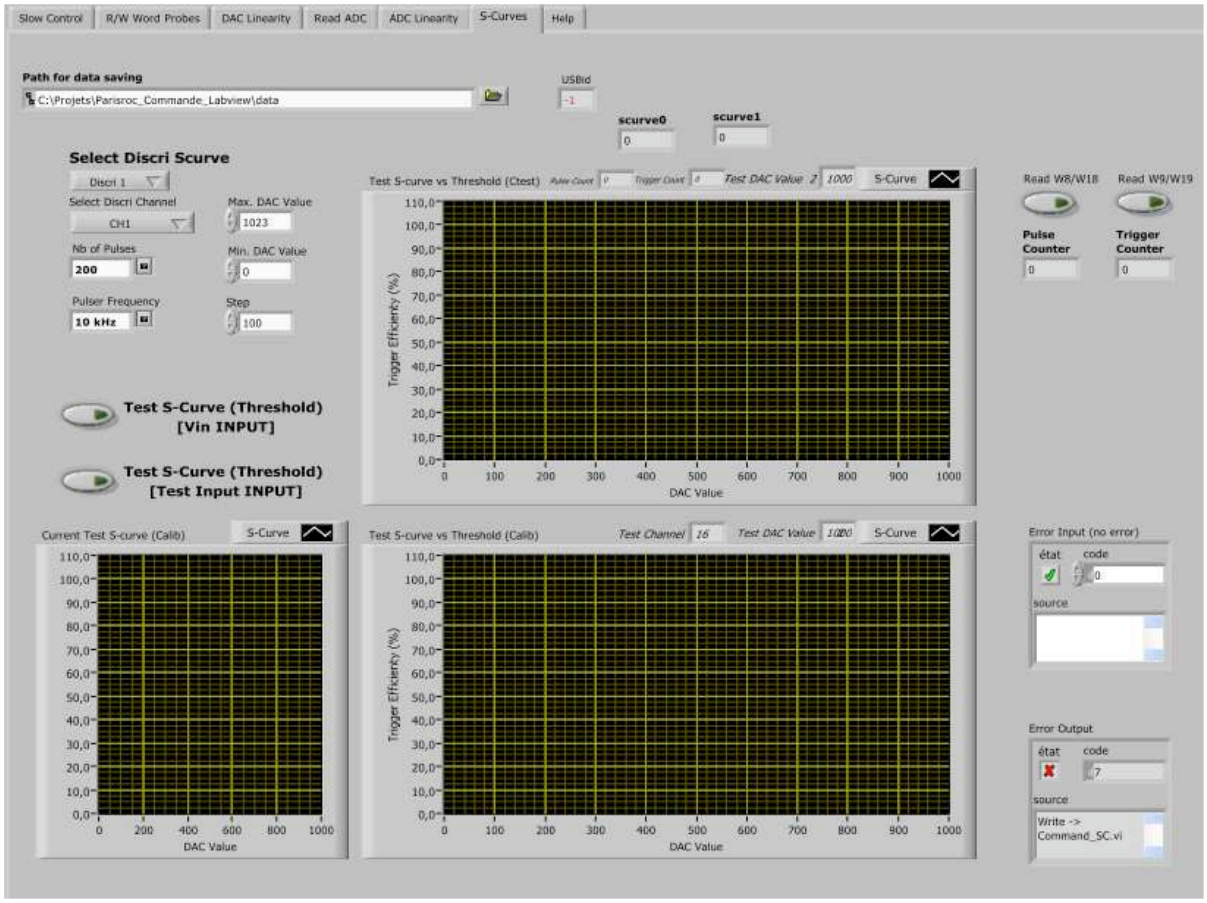

Figure 3.8. Labview S-Curve tab.

2.3. Input signal

A single channel function generator is used to create the input charge injected in the ASIC. The signal has the shaping, as similar as possible, to the PMT signal. In Figure 3.9 is represented the generator signal used for measurements.

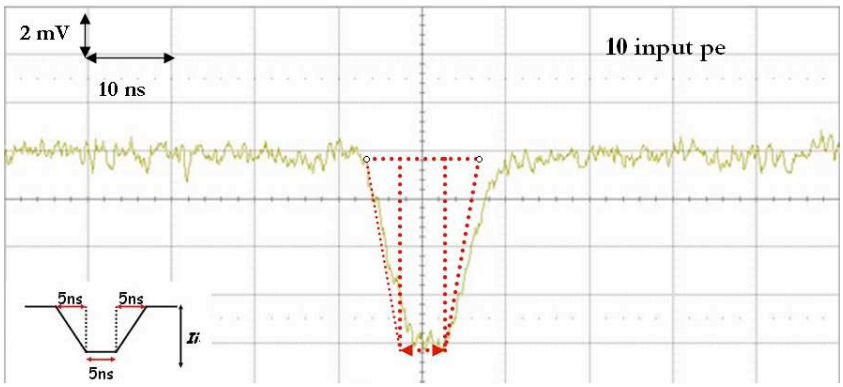

Figure 3.9. Input signals. A single channel function generator is used to create the input charge injected in the ASIC. The shaping is as similar as possible to the PMT signal.

This input signal can be seen as a negative triangular signal with a rise time, pulse width and fall time of 5 ns.

The input dynamic range required by the project is from 50 fC and 50 pC (from 1/3 to 300 p.e.) at a PMT gain 10^6.
From the shape of the input signal the range of the current that flows in the chip is calculated from 5 µA to 5 mA. Therefore, with an input resistor of 50 Ω, put on the board, the voltage input dynamic range is from 250 µV to 250 mV.
A signal of 250 mV is set on the pulse generator. It corresponds to an input charge of 300 photoelectrons that can be varied thanks to an attenuator put between the pulse generator and the board.
Figure 3.9 shows that the injected signal used for most measurements doesn't have the shape exactly equal to the one used in simulation (Figure 2.16 in Chapter II). Therefore, this different input signals can affect the results obtained in measurements and simulations and then their comparison, described in the next sections, that will exhibit small differences.

3. Analog part tests

The ASIC measurements start with the verification of the power dissipation (12 mW per channel), the chip dc levels on each pin and the analog signals pedestals. The ASIC has a dedicated output pin that allows to observe the output analog signals selected. The selection is made by the probe register (Annex II) set by the Labview program (Figure 3.4).
Figure 3.10 shows the chip pin out composed of 160 pins divided into analog (for analog bias and voltage analog references), power supply (Vdd and gnd) and digital pins (complete pin list is in the Annex III). All the pins voltage levels are tested before starting the other measurements. Good values are obtained comparing to the simulation values.

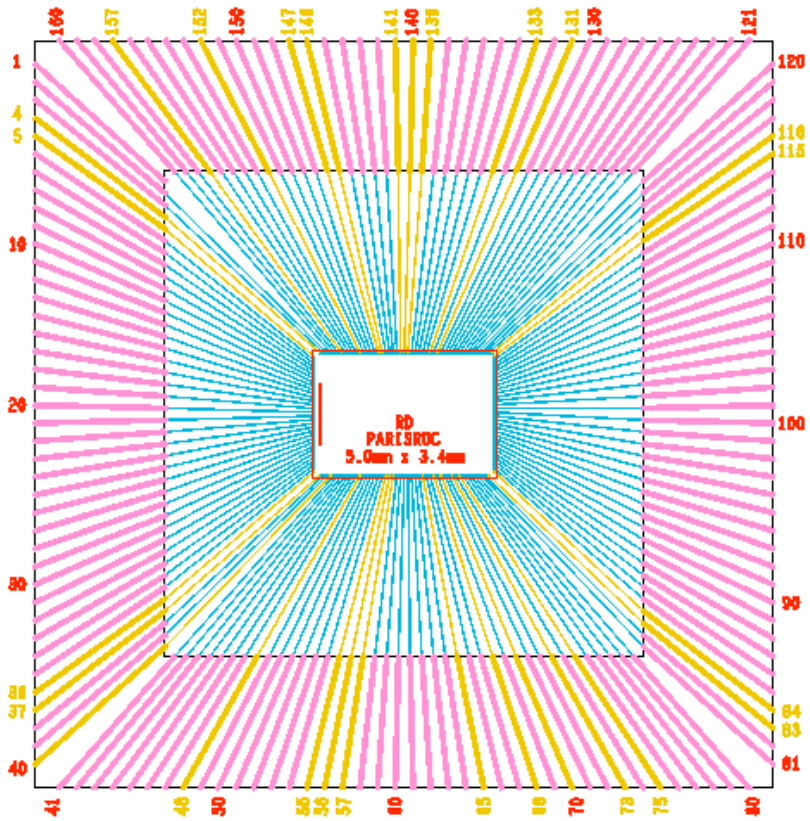

Figure 3.10. PARISROC pin-out.

The DC levels, named also Pedestals, of each analog output signals, for all channels, are measured.
Figure 3.11, Figure 3.12 and Figure 3.13 respectively give the preamplifier, slow shaper and fast shaper pedestals uniformity plots for the 16 channels. Table 3.1 summarized the performances obtained.

A small dispersion of 0.4%, 0.1% and 0.05% has been obtained respectively for the preamplifier, the slow shaper and the fast shaper corresponding to the expected offset of these stages.

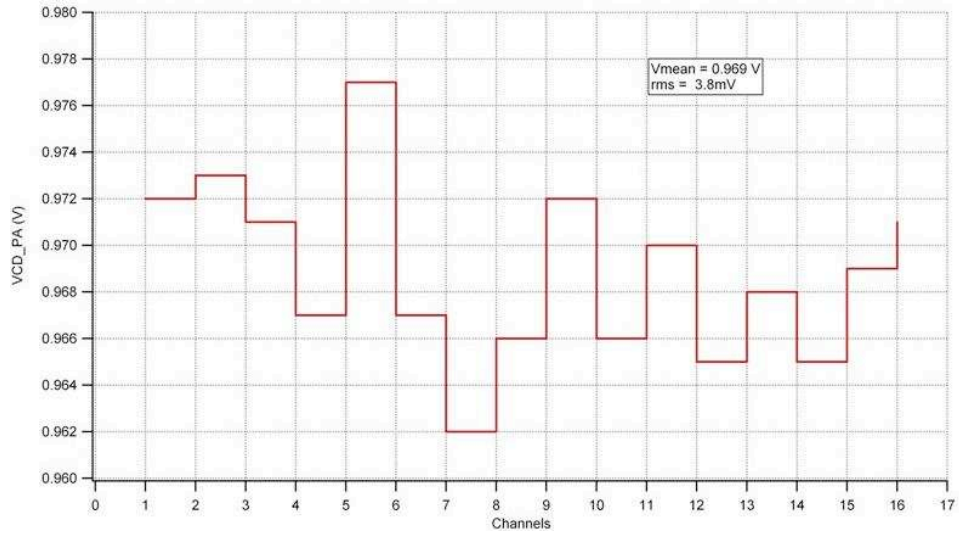

Figure 3.11. Pedestal uniformity. Preamplifier DC level vs channel number.

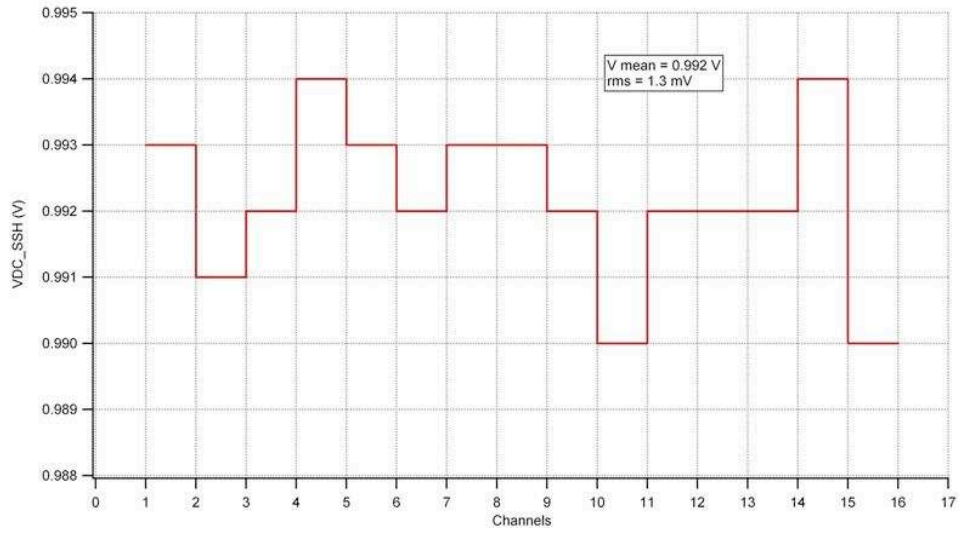

Figure 3.12. Pedestal uniformity. Slow shaper DC level vs channel number.

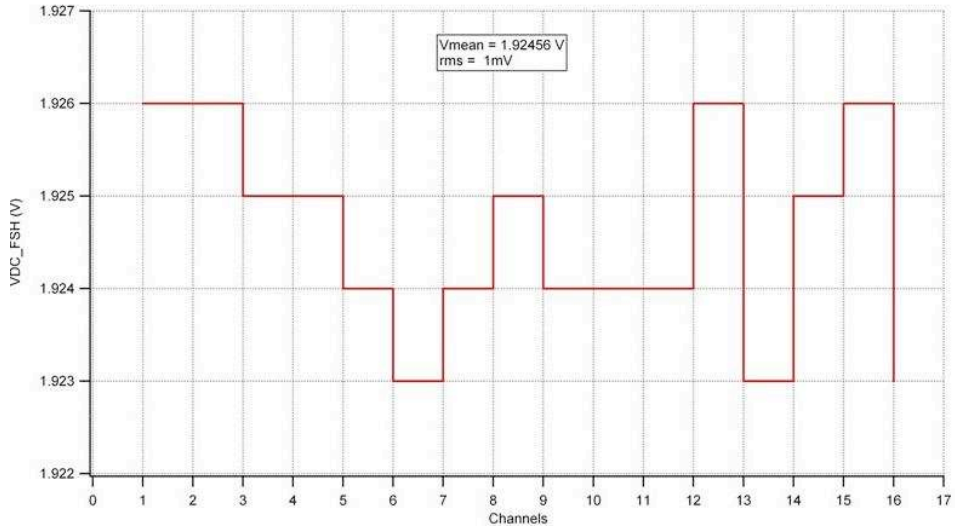

Figure 3.13. Pedestal uniformity. Fast shaper DC level vs channel number.

	Mean DC level (V)	Rms (mV)	Rms %
Preamplifier	0.969	3.8	0.4
Slow shaper	0.992	1.3	0.1
Fast shaper	1.92	1	0.05

Table 3.1. Analog part Pedestal uniformity.

3.1. Analog output signals

The DC tests are followed by the verification of the analog signals: the board is connected to the pulse generator, to a PC running the test program (Labview) and to the oscilloscope. Injecting different input charges, the preamplifier, slow shaper and fast shaper output waveforms are observed and measured (with the oscilloscope) to be compared with the simulation results.

3.1.1. Preamplifier

Injecting a charge equivalent to 10 p.e. at a PMT gain of 10^6 (input voltage signal of 8 mV) and setting a preamplifier gain[48] at 8, the preamplifier output signal has amplitude of 50 mV. In figure 3.14 are shown the preamplifier output waveforms obtained in measurement (on the left) and in simulation (on the right). The simulation results indicate that the preamplifier amplitude is of 56 mV for the same injected charge, in reasonable agreement with measurements.

[48] The input capacitor, Cin, is set at 4pF and the feedback capacitor, Cf, at 0.5 pF

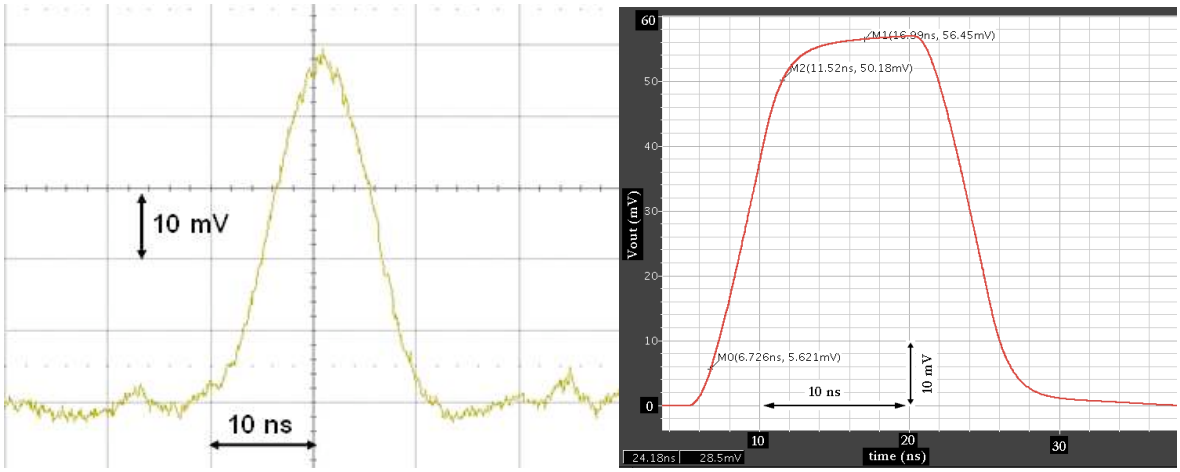

Figure 3.14. Measurement and simulation of the preamplifier output for an input charge of 10 p.e and gain 8. Voltage level (mV) versus time (ns) is plotted.

Table 3.2 lists the preamplifier signal characteristics for measurements and simulations; a difference of 10% in amplitude and 3 ns in rise time[49] has been observed in comparison to the simulations.

	Preamplifier maximum voltage (mV)	**Rise time (ns)**	**Difference in amplitude**
Measurement	~ 50 mV	~ 7.8 ns	11 %
Simulation	56.45 mV	~ 5 ns	

Table 3.2. Preamplifier results for an input charge of 10 p.e; and gain 8.

A buffer is placed on the test board between the ASIC output and the oscilloscope; different shapes have been observed before or after the buffer. In Figure 3.15 are illustrated the two signals with evident differences in amplitude and rise time. This discrepancy will be present for all the analog signals.

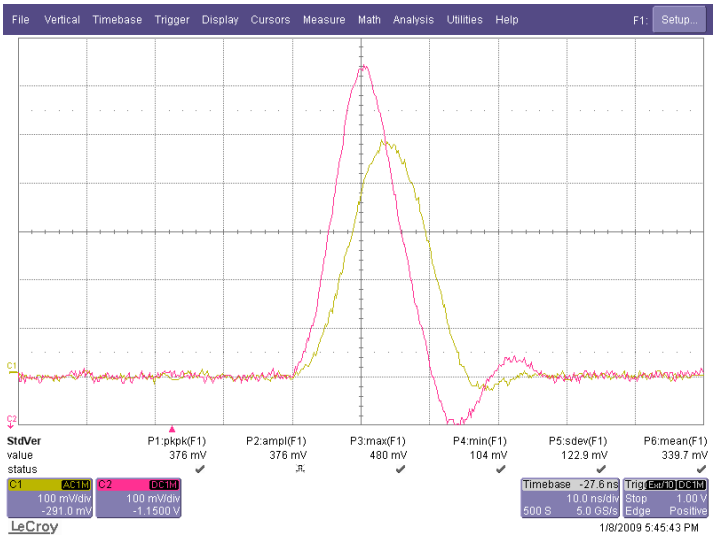

Figure 3.15. Preamplifier output signals. The yellow and pink curves represent the preamplifier waveforms respectively after and before the buffer.

Figure 3.16 and Table 3.1 show the preamplifier characteristics for an injected charge of 1 p.e. The measured signal with 5 mV amplitude is visualized on the left panel and compared on the right panel to the simulation result with amplitude of 5.43 mV.

[49] Measured as the time required for the signal to change from the 10% and the 90% of the maximum value.

The one p.e. input charge will be a reference signal in all the measurements described in the next paragraphs.

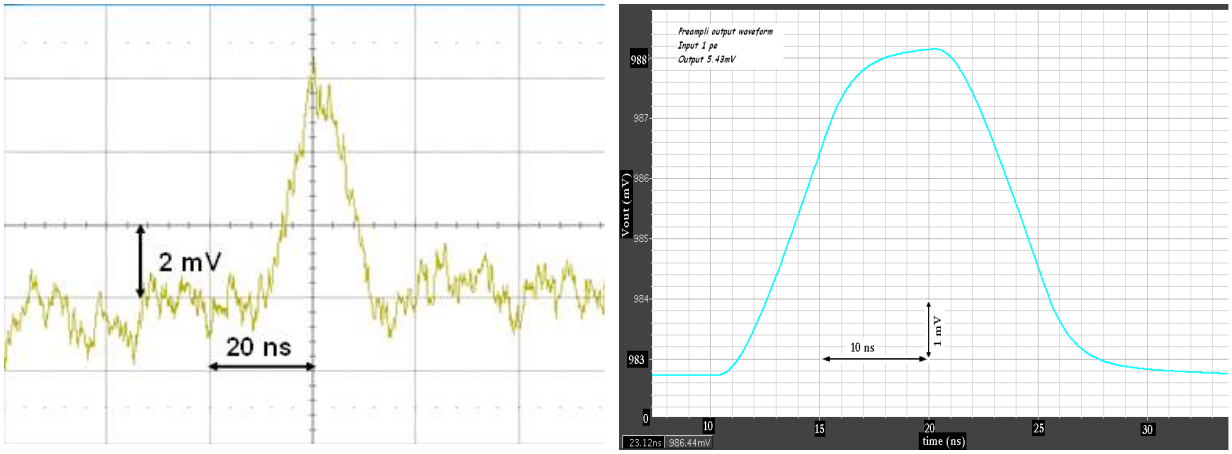

Figure 3.16. Measurement and simulation of the preamplifier output waveform for an input charge of 1 p.e. and gain 8; the measured signal is not averaged to show the noise level.

	Preamplifier maximum voltage (mV)
Measurement	~ 5 mV
Simulation	5.43 mV

Table 3.3. Preamplifier results for an input charge of 1 pe and gain 8.

3.1.2. Slow shaper

The slow shaper output signal, for a settled shaping time of 50 ns and a preamplifier gain at 8, evidences the same difference observed on preamplifier; for an input signal of 10 p.e. the measurements and simulations results gives 35 % of difference in amplitude (Figure 3.17 and Table 3.4). This large percentage comes from the output buffer, as explained previously, but also from the shape of the input signal. As seen in the previous chapter, the response of a filter depends directly on the shape of the input signal in terms of maximum output voltage, rise time etc. Therefore the input signal measured is slower than one simulated (Figure 3.14) and it explains the important difference measured at the slow shaper output.

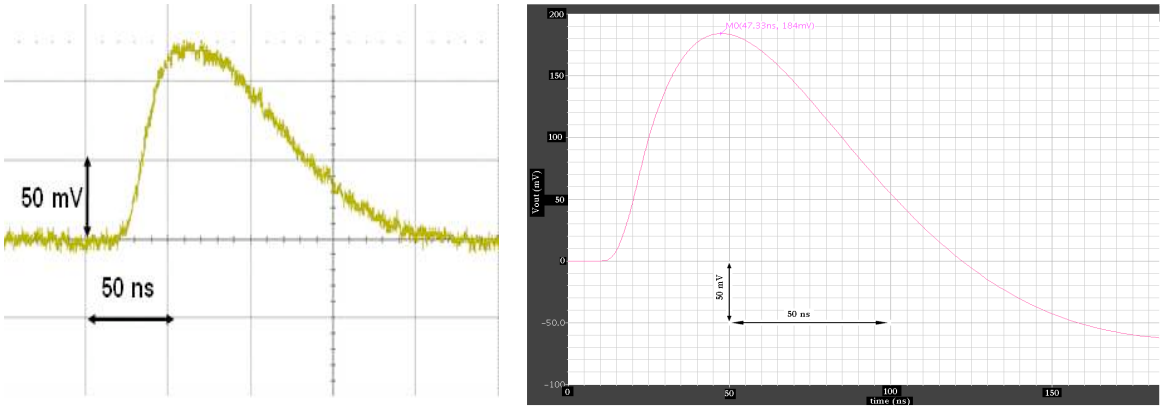

Figure 3.17. Measurement and simulation of the slow shaper output signal for an input charge of 10 p.e. and shaping time of 50 ns for a preamplifier gain of 8.

	Slow shaper maximum voltage (mV)	Rise time (ns)	Difference in amplitude
Measurement	~ 120 mV	~ 18 ns	38 %
Simulation	194 mV	~ 19 ns	

Table 3.4. Slow shaper results for an input charge of 10 p.e. and shaping time of 50 ns for a preamplifier gain of 8.

Figure 3.18 illustrates the slow shaper responses for an injected charge of one p.e. and 50 ns of shaping time. On the left and right are respectively displayed the slow shaper signals for measurement (12 mV amplitude) and simulation (15 mV amplitude). And Table 3.5 lists the shaper response at 1 p.e. for various shaping time.

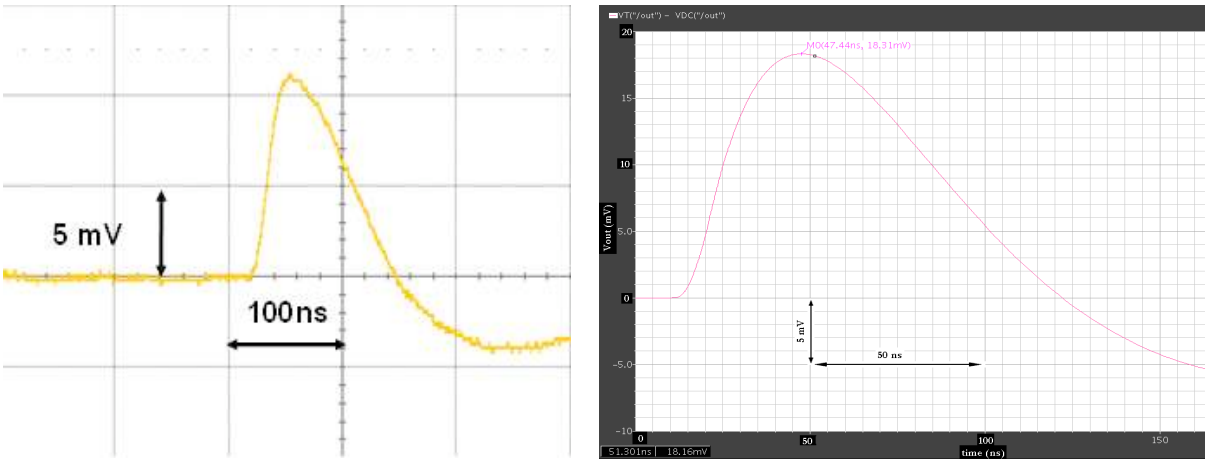

Figure 3.18. Measurement and simulation of the slow shaper output for an input charge of 1p.e. and shaping time of 50 ns for a preamplifier gain of 8; the measured signal is averaged.

Shaping time	Slow shaper maximum voltage in measurement	Slow shaper Maximum voltage In simulation	Difference in amplitude %
50ns	12 mV	19 mV	37 %
100ns	7.5 mV	10 mV	25 %
200ns	5 mV	5 mV	0

Table 3.5. Slow shaper results for an input charge of 1 p.e. and variable shaping for a preamplifier gain of 8.

3.1.3. Fast shaper

The fast shaper response for an injected charge of 10 p.e. and with a preamplifier gain of 8 is shown in Figure 3.19 on the left panel, this measurement evidence amplitude of -220 mV that is compared with the simulation result, displayed on the right panel, with amplitude of -400 mV. Therefore the two results have a difference of 45 % that can be explained with the same arguments as the slow shaper and this difference is more important as the shaping is faster.
Table 3.6 lists the fast shaper characteristics.

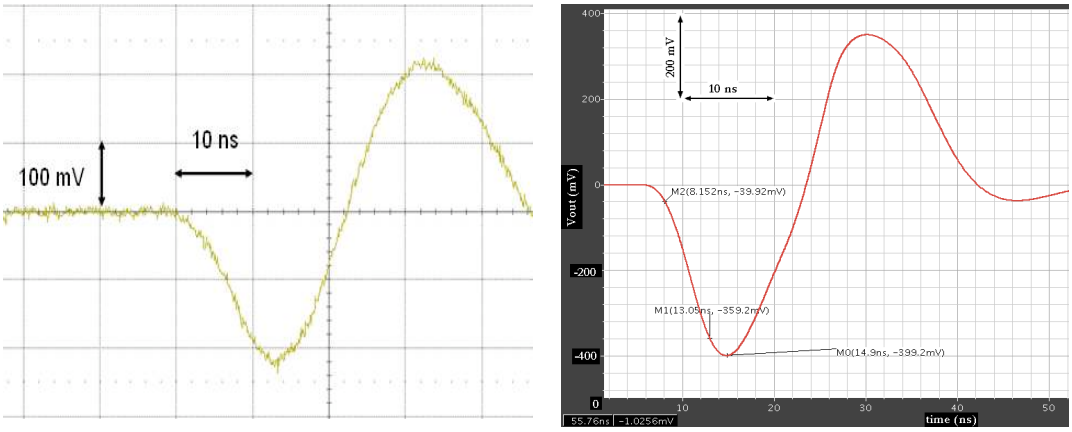

Figure 3.19. Measurement and simulation of the fast shaper output for an input charge of 10 p.e and preamplifier gain of 8.

	Fast shaper maximum voltage (mV)	Rise time (ns)	Difference in amplitude
Measurement	~ - 220 mV	~ 7 ns	45 %
Simulation	- 400 mV	~ 5 ns	

Table 3.6. Fast shaper results for an input charge of 10 p.e and preamplifier gain of 8.

With a charge of 1 p.e. the fast shaper response gives a signal of 30 mV in amplitude (Figure 3.20 on the left) that is 21 % smaller than the value obtained in simulation and shown on the right panel of Figure 3.20. Table 3.7 lists the fast shaper parameters.

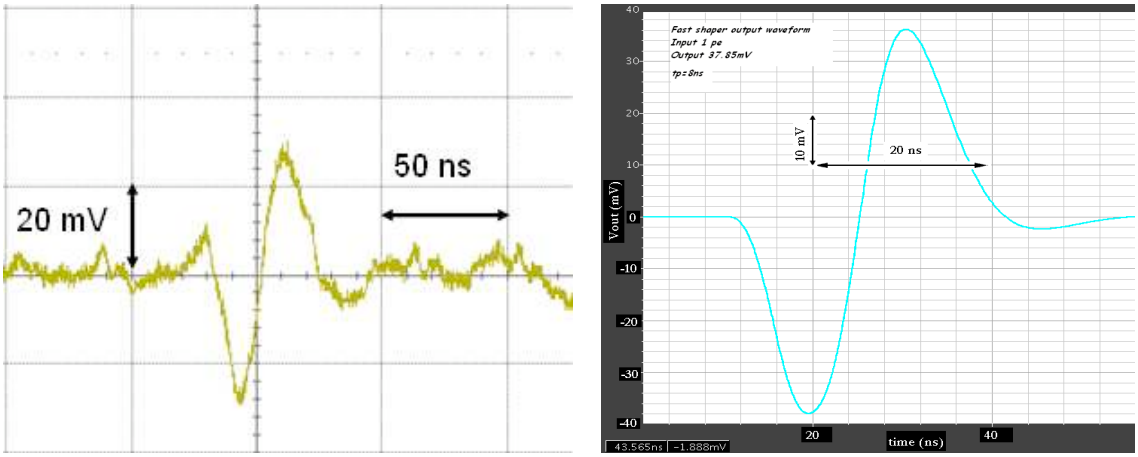

Figure 3.20. Measurement and simulation of the fast shaper output for an input charge of 1 p.e. and preamplifier gain of 8; the signal is not averaged to show the noise level.

	Fast shaper maximum voltage (mV)	Rise time (ns)	Difference in amplitude
Measurement	~ - 30 mV	~ 6 ns	21 %
Simulation	- 38 mV	~ 5 ns	

Table 3.7. Fast shaper results for an input charge of 1 p.e. and preamplifier gain of 8.

3.2. Linearity

The linear response at each charge injected is an important characteristic that described the input-output relationship of the circuit. In order to study it, the maximum voltage value of each analog output signal is usually plotted as a function of the input injected charge and a linear fit is performed. It can also be represented as a function of other parameters such as the gain.

3.2.1. Preamplifier linearity

Figure 3.21 gives a few examples of the preamplifier linearity at different preamplifier gains (8, 4 and 2) and Table 3.8 summarizes the fit results of the linearity.
The three plots show respectively the linearity for a preamplifier gain of 8 in the top panel, gain 4 in the middle panel and gain 2 in the bottom panel. Good linearity is obtained respectively with residuals better than the 1.2% until 80 p.e. for gain 8; 1.7% until 200 p.e. for gain 4 and 2% until 300 p.e. for gain 2.
Comparing the measurements and the simulation results (§ 3.2.2 Chapter II, figure 2.18 and table 2.3) it can be observed that the preamplifier is more linear in simulation with a larger dynamic range until 250 p.e. for gain 8 and until 300 p.e. for gain 4 and 2.

Preamplifier Gains	**Maximum voltage (V)**	**Maximum Charge (C) (Number of p.e.)**	**Residuals** %
8	0.52	12 pC (78 p.e.)	-1.2 to 0.8 %
4	0.64	32 pC (198 p.e.)	-1 to 1.7 %
2	0.51	50 pC (312 p.e.)	-2 to 1.5 %

Table 3.8. Fit results for preamplifier linearity.

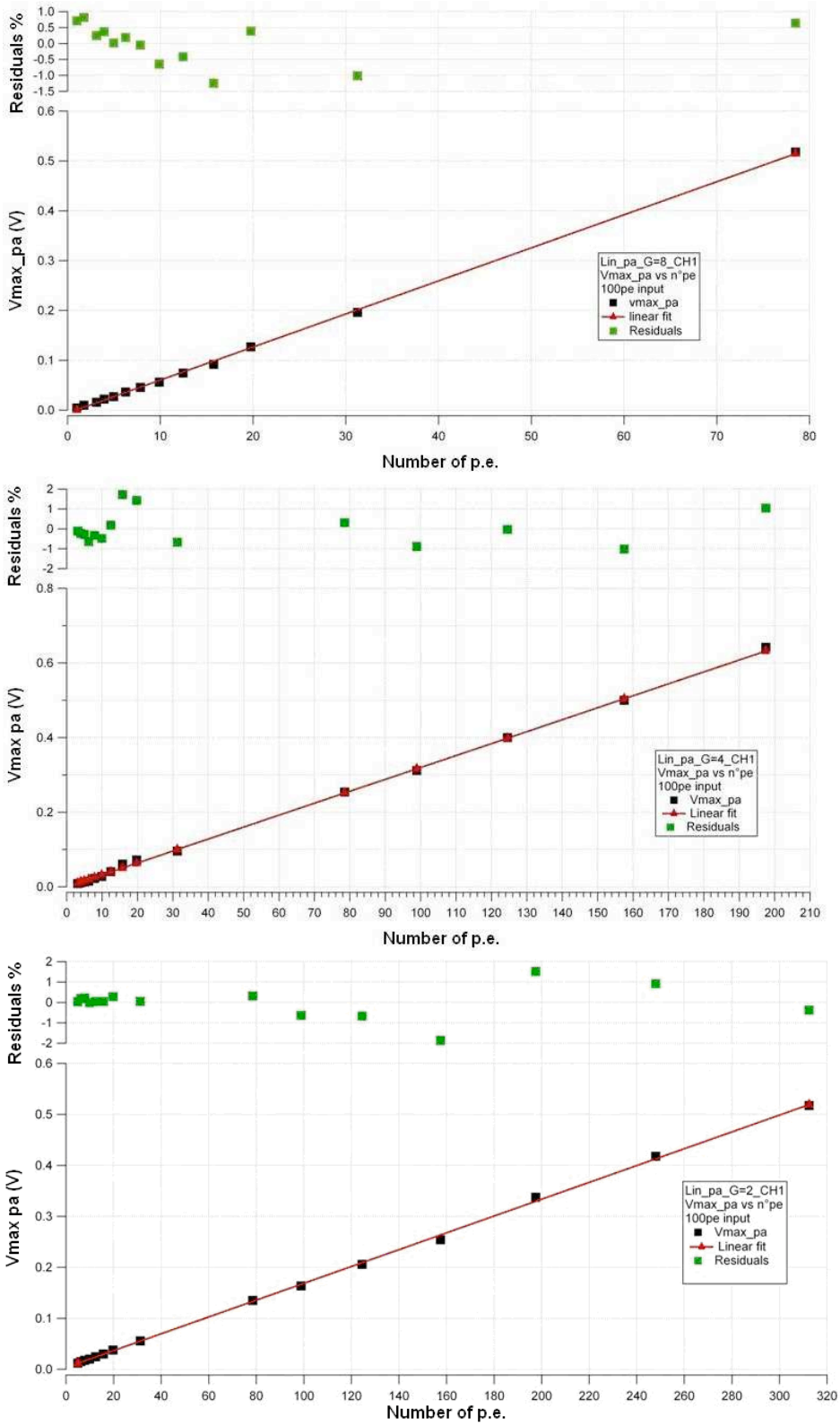

Figure 3.21. Preamplifier linearity versus injected charge for different gains. The top plot for gain 8; middle plot for gain 4 and the bottom plot for gain 2.

3.2.2. Slow shaper linearity

An example of slow shaper linearity is shown in Figure 3.22; with a preamplifier gain of 8 and the slow shaper shaping time of 50 ns. A good linearity is reached, until 100 pe, with residuals from -0.8% to 0.8%.

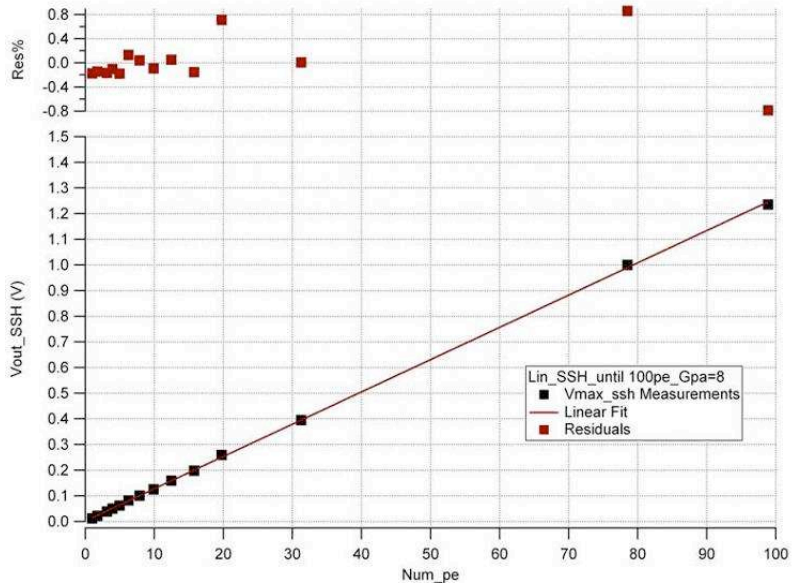

Figure 3.22. Slow shaper linearity versus injected charge for shaping time of 50 ns and a preamplifier gain of 8.

3.2.3. Fast shaper linearity

The fast shaper linearity has been investigated up to an injected charge of 10 p.e. for a preamplifier gain of 8 (Figure 3.23)
Residuals better than ± 2% are obtained. The linearity study has been restricted to small input signals because of the fast shaper saturation. The goal of the fast shaper is not to be linear but to have high gain in order to be discriminated easily.

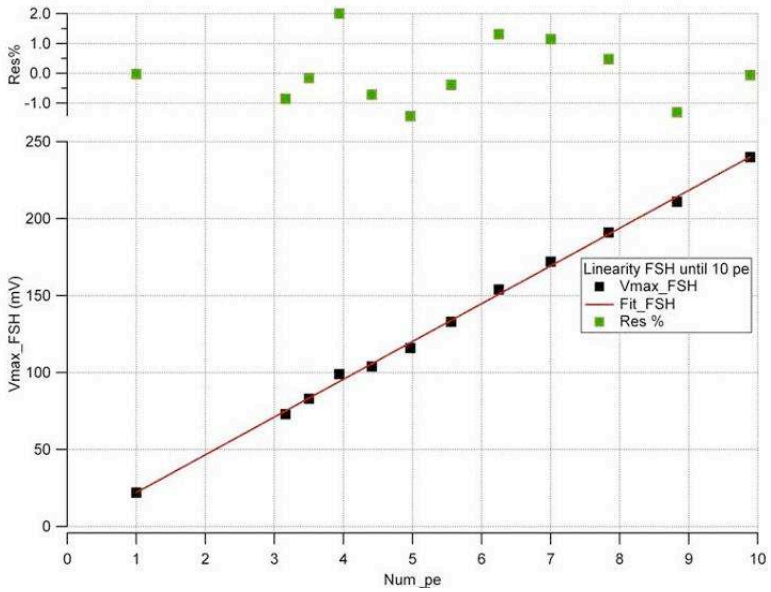

Figure 3.23. Fast shaper linearity versus injected charge for a preamplifier gain of 8 and until 10 p.e.

3.2.4. Further studies with the preamplifier

The behavior for small input signals has been checked for the preamplifier while scanning the variable feedback capacitor values. This is a way to study the linearity as a function of the gain[50].
The linear fit and its residuals (from -2.5% to 1.35%) are represented in Figure 3.24; the measurements indicate a kind of gain adjustment linearity, that is good to 2% on 8 bits.

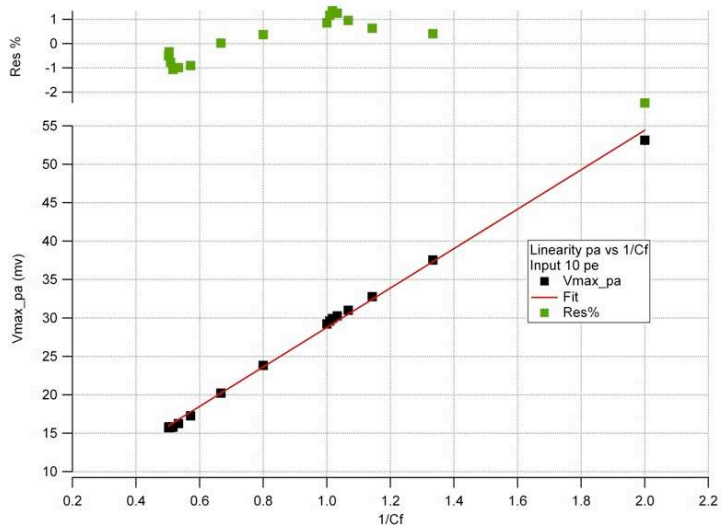

Figure 3.24. Preamplifier linearity vs feedback capacitor value.

A study of the gain uniformity has been done for all 16 channels. For the different preamplifier gains is plotted the preamplifier maximum voltage value for all channels in order to investigate the homogeneity among the whole chip, essential for a multichannel ASIC.
On Figure 3.25 are displayed the gain uniformity plots for an input signal of 100 p.e. with a fixed Cin value of 4pF and a variable Cf value. An important signal is injected in the input to simplify the measurements. A nice dispersion of 0.5%, 1.4% and 1.2% are, respectively, obtained for gain 8, 4 and 2. This matches a goal of the ASIC.

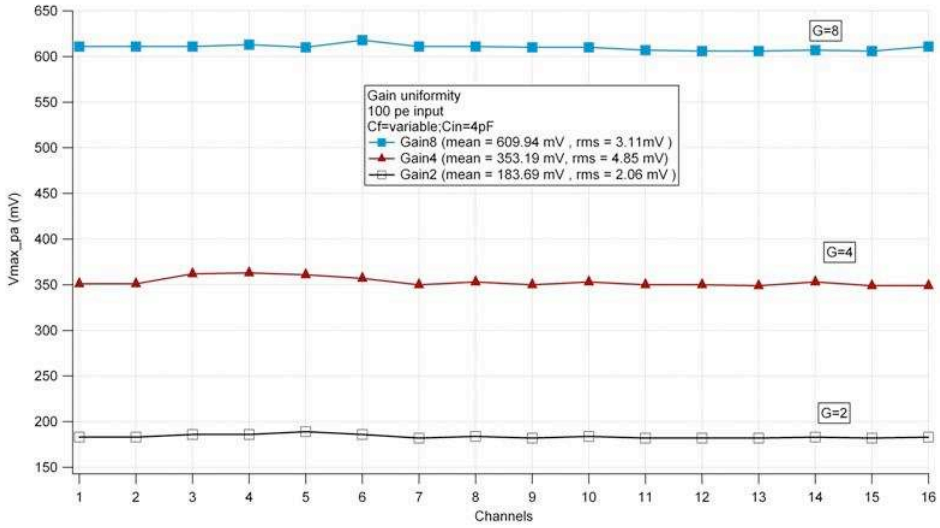

Figure 3.25. Gain uniformity for Gpa=8, 4, 2 obtained chancing the Cf value; preamplifier maximum output voltage versus channels.

[50] Preamplifier gain is equal to $\frac{Cin}{Cf}$; with a fixed value of Cin the maximum value of the output signal is proportional to $\frac{1}{Cf}$.

Equally on Figure 3.26 are shown the gains uniformity for the same input signal (100 pe) but with a fixed Cf value of 0.5 pF and a variable Cin value. Dispersions of 0.27% for preamplifier gain 8, 0.76% for gain 4 and 0.9% for gain 2 are obtained.

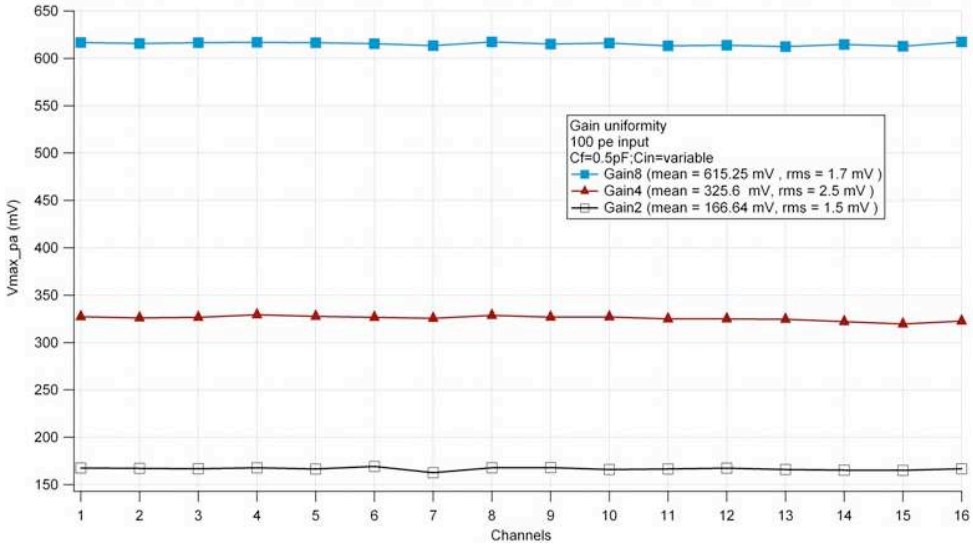

Figure 3.26. Gain uniformity for Gpa=8, 4, 2 obtained chancing the Cin value; preamplifier maximum output voltage versus channels.

These measurements are evaluated also plotting the maximum voltage values versus the different gains for the 16 channels; these curves must be linear. In Figure 3.27 are shown the plots with Cin fixed and Cf variable for the 16 channels with their fits (red curve).

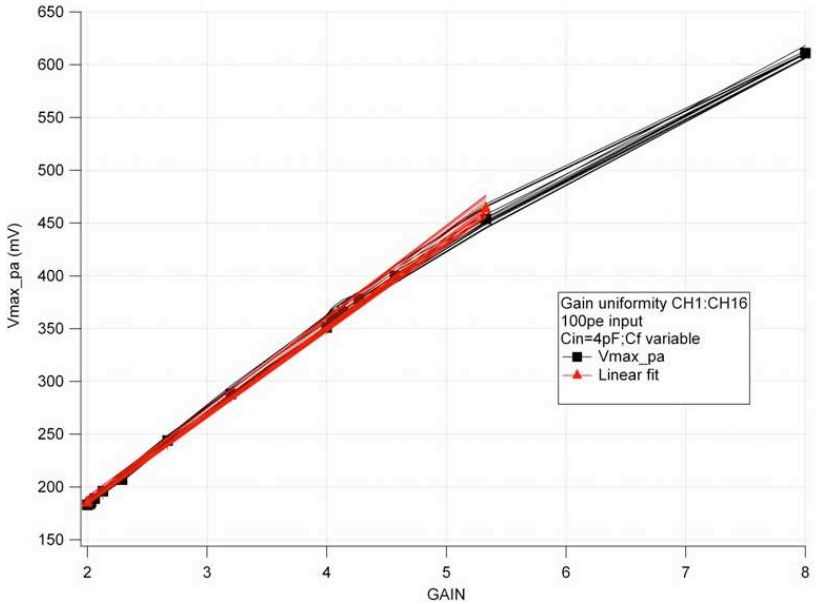

Figure 3.27. Linear fits. Cin=4pF and Cf variable. Preamplifier maximum output voltage versus preamplifier gains for the 16 channels.

The slopes and the intercepts for each fit are studied: the distributions of these two parameters give an estimate. On Figure 3.28 are represented these two parameters. Rms values of 2 for intercept and 1.47 for slope indicate a good uniformity.
The curves on Figure 3.27 are fitted until gain 6 because of the large input signal that brought to the preamplifier saturation for high gains.

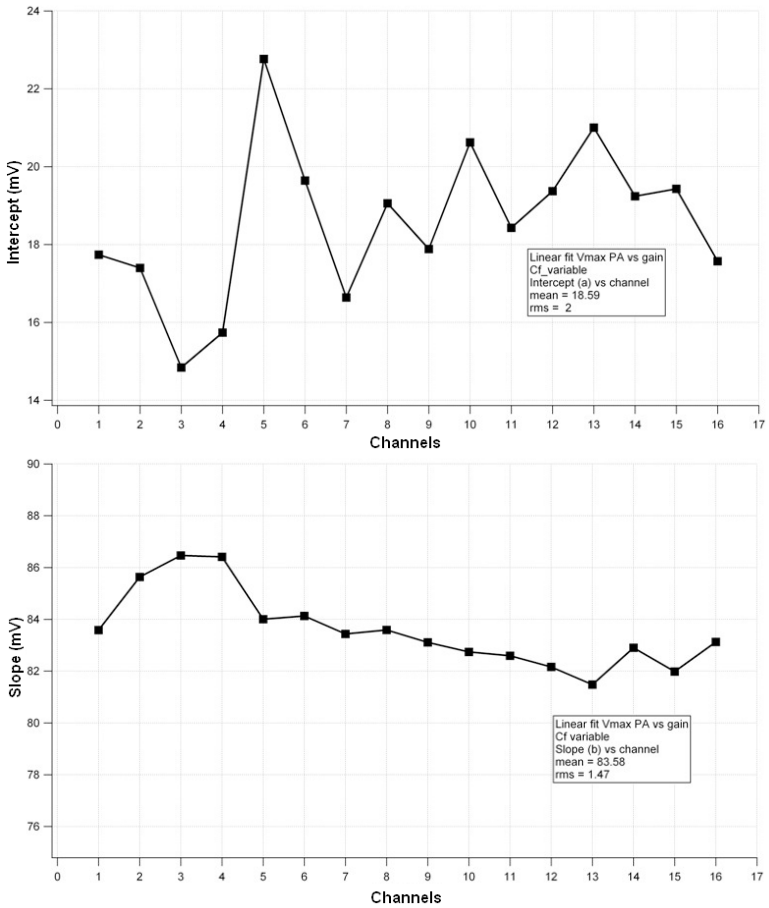

Figure 3.28. Intercept and slope. Cin=4pF and Cf variable.

The same study has been done for the curves obtained changing Cin and with Cf fixed. In Figure 3.29 are shown the plots for the 16 channels with theirs fits and on Figure 3.30 are represented the intercept and the slope as a function of the channel number. Rms values of 1.48 mV for intercept and 0.24mV for slope indicate a good uniformity. The better uniformity, in this case, until high gains, is due to the fact that it has been calculated only for three values: Cin=1pF, 2pF and 4pF.

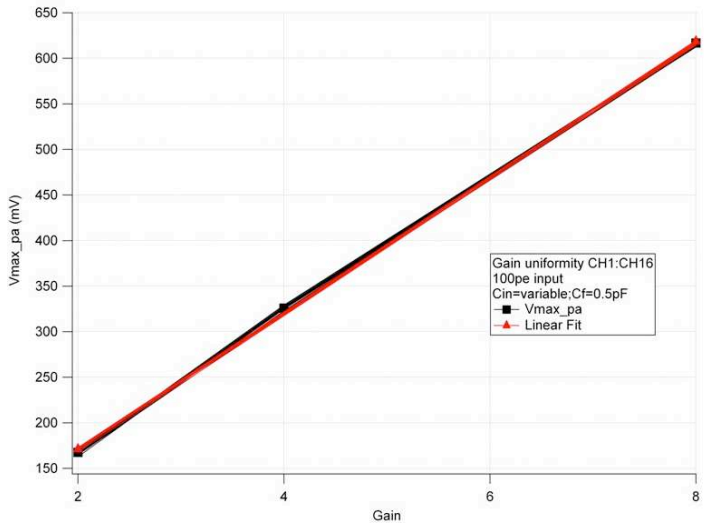

Figure 3.29. Linear fit. Cin variable and Cf=0.5 pF.

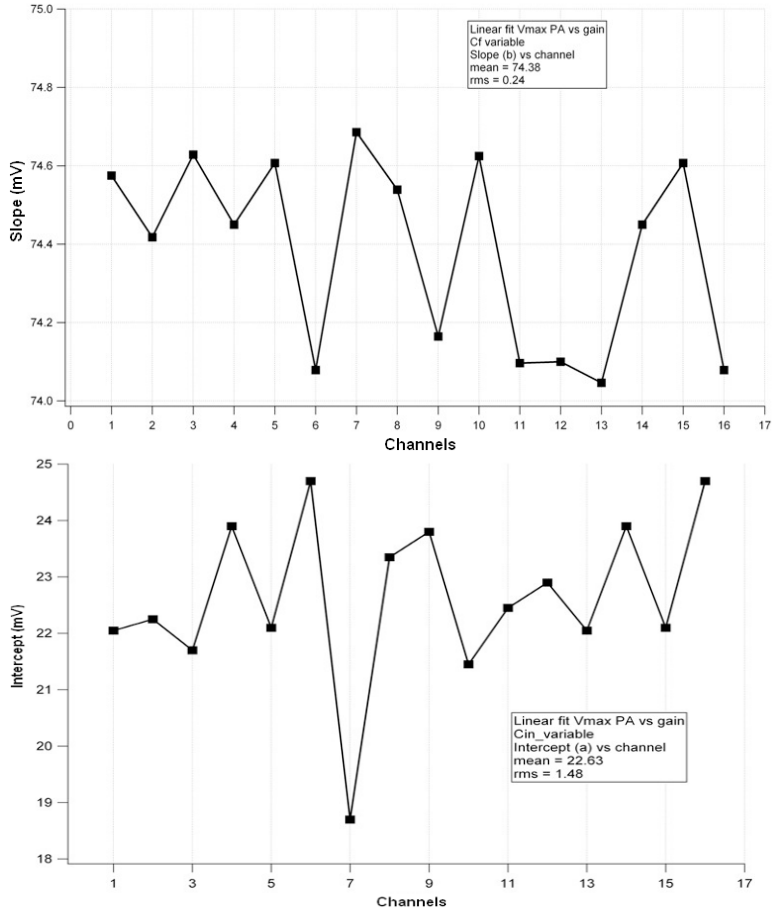

Figure 3.30. Intercept and slope. Cin variable and Cf=0.5pF.

3.3. Conclusion preliminary tests

The preliminary tests, for the ASIC PARISROC, have shown good DC pins levels and very good pedestal dispersion with a maximum value of 0.4% for the preamplifier.
The analog responses of the three main analog cells (preamplifier, slow shaper and fast shaper) have been shown differences in amplitude on the output analog signals, in comparison to simulations results. This characteristic is due to the output buffer that is not capable of following the input signal (the buffer bandwidth is not enough).
The slow shaper and fast shaper amplitudes have different values for more reasons:

- The output buffer;
- The strong dependence of a filter response to the shape of the input signal: simulation and measurement input signals don't have exactly the same shape;
- The output signals are measured thanks to the analog output probe[51] that selects the analog output signal that must be tested; this probe add output capacitive load to the analog cell that can change the shape of the analog signals.

The preliminary tests show, also, a good linearity of the three main analog cells and a good gain uniformity, important for a multichannel chip.

[51] Which is a switch controlled by probe register.

4. Noise measurements

Noise measurement is an important step in laboratory ASIC tests thus each analog cell has been studied in terms of noise. It was calculated on the oscilloscope without injecting input signal. The oscilloscope rms noise is of order 300 μV without any connection with the board and the cables. This value will be subtracted in quadrature from all the rms noise values measured for each analog component.
Setting the preamplifier gain at 8 by slow control, the rms noise values are annotated for each analog cell. In Table 3.9 are listed the rms noise values observed on the preamplifier, slow shaper and fast shaper outputs. These measurements show:

- A noise contribution more important compared to the simulation;
- A strange peak to peak value of the DC level;
- An incorrect correlation between the slow shaper rms noise and the shaping time.

These results depend on the clock noise as demonstrated and explained in § 4.1 Chapter III.
Investigations followed to find explanations of this higher noise brought us to perform similar measurements without the USB cable that connects the board to the PC: the rms value is of 660 μV for preamplifier, 3.5 mV for slow shaper (τ=50ns) and 2.3 mV for fast shaper therefore this USB cable injects an extra noise in the test board.

Preamplifier gain 8	**RMS noise measurement (@ 100 μs)**	**RMS noise simulation**	**peak to peak value**
Preamplifier	1 mV	468 μV	11mV
Slow shaper			
50ns	4 mV	1.68 mV	
100ns	6 mV	1.2 mV	40 mV
200ns	10 mV	0.980 mV	
Fast shaper	2.5 mV	2.36 mV	25 mV

Table 3.9. Noise measurements and simulations.

Table 3.10 shows the signal to noise ratio (SNR) for each analog cell. The signal used to calculate this quantity is 1 p.e. that is the minimum input signal to detect. The SNRs obtained in measurement have smaller values than those expected from simulation, in particular for the slow shaper.

Preamplifier gain 8	**Maximum voltage at 1 p.e. measurement**	**S/N measurement**	**Noise in number of p.e. measuremant**	**Maximum voltage at 1 p.e. simulation**	**S/N simulation**
Preamplifier	5 mV	5	0.2 pe	5.43 mV	11.6
Slow shaper					
50ns	12 mV	3	0.3 pe	19 mV	11.3
100ns	7.5 mV	1.25	0.8 pe	10 mV	8.3
200ns	5 mV	0.5	2 pe	5 mV	5
Fast shaper	30 mV	12	0.08 pe	37 mV	15.6

Table 3.10. 1p.e. analog cell responses; Signal to noise ratio @ 1 p.e. and noise in number of photoelectrons. Measurements and simulations.

To study these SNRs values, the fast shaper output signals and its rms noise values are measured changing the preamplifier gain through the input and feedback capacitors. The injected charge is 3 p.e. The fast shaper output amplitudes, the output noise and the signal to noise ratio are listed in Table 3.11. The SNR values are plotted versus the Cf and Cin values (Figure 3.31).

Cin \ Cf	0.25 pF	0.5 pF	1 pF
2 pF	Vout = 63 mV RMS = 4.46 mV S/N = 14.12	Vout = 35.8 mV RMS = 2.9 mV S/N = 12.34	Vout = 22 mV RMS = 2 mV S/N = 11
4 pF	Vout = 123 mV RMS = 4.9 mV S/N = 25	Vout = 73 mV RMS = 3.8 mV S/N = 19.21	Vout = 38 mV RMS = 3.4 mV S/N = 11.18
7 pF	Vout = 210 mV RMS = 4.6 mV S/N = 45.65	Vout = 125.5 mV RMS = 3.8 mV S/N = 33.03	Vout = 68.5 mV RMS = 3.3 mV S/N = 20.75

Table 3.11. Signals and the rms noise values at fast shaper output for input signal of 3 pe and different Cf and Cin values.

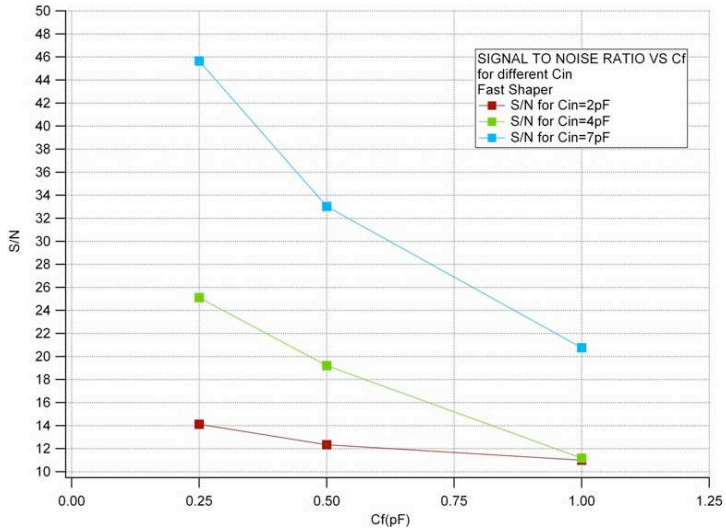

Figure 3.31. Signal to noise ratio observed at fast shaper output for input signal of 3 p.e. and different Cf and Cin values.

These curves trend were expected considering that, for higher gain the signal to noise ratio is higher. The strangeness is in the rms values that change with Cf whereas there are small changes with Cin.
This behaviour is confirmed testing the preamplifier noise by an external shaper ($CRRC^2$). The preamplifier output signal is injected in the input of this external (to the chip) shaper and, changing the shaping time, the shaper rms values are observed for two preamplifier gains.
The rms noise values measured are plotted versus the variable shaping time for preamplifier gain 8 and 14 (obtained with Cf fixed to 0.5 pF and Cin 4 pF and 7 pF) and shown in Figure 3.32. The picture indicates that the parallel noise and the series noise are respectively dependent and independent of Cin. Theoretically it should be the opposite, the parallel noise should not depend on Cin (whereas from Cf) and the series noise should depend on Cin.
This behavior is due to the structure of the Cin: when one Cin value is selected, one switch is closed and the others are opened; the open switches are connected to the supply (VDD) so:

- The others two input capacitors value became parasitic capacitors in series noise calculation, like the input capacitor was always at 7 pF (Figure 3.33). This justifies the independence of the series noise by Cin (contrarly to the theory).
- The extra parallel noise (that is dependent by Cin) is due to the noise injected by the positive power supply in Cin. This behavior was expected by the simulation as explained in § 3.5.1 of Chapter II.

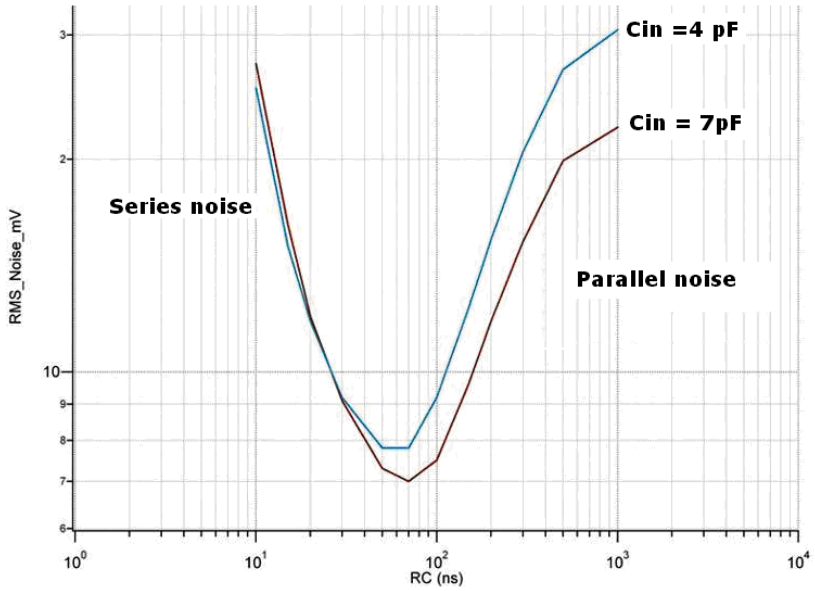

Figure 3.32. External slow shaper rms noise values for Cin_pa=4 pF (blue) and Cin_pa=7 pF (red) versus shaping time.

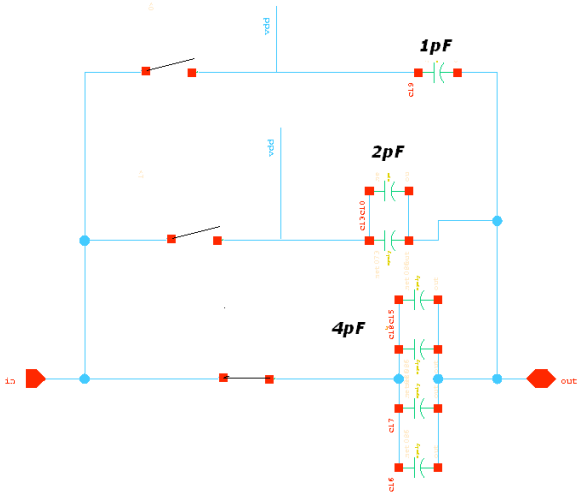

Figure 3.33. Preamplifier input capacitor (Cin) structure.

A comparison of measurements performed with external and internal shaper is carried out setting a preamplifier gain of 14, to have a better signal to noise ratio, and selecting a step signal on the pulse generator with attenuation of 66 dB i.e. 0.132 mV in preamplifier input.
With the shaping time of 50 ns the external shaper gives a maximum voltage value of 125 mV and an rms noise of 10.2 mV.
Therefore the number of injected electrons is:

$$N°e^{-}injected = \frac{Q_i}{Q_{e^-}} = \frac{Vi * Cin}{Q_{e^-}} \qquad (3.\ 1)$$

With $Q_{e^-} = 1.6*10^{-19} C$ and Cin=7 pF

$$N°e^{-}injected = \frac{0.132mV * 7pF}{1.6*10^{-19} C} = 5775e^{-} \qquad (3.\ 2)$$

And the ENC:

$$ENC = \frac{Vn}{Vout} * \left(N°e^{-}injected\right) = 471e^{-} \qquad (3.\ 3)$$

The same measurement is performed with the internal shaper, injecting a step of 1.25 mV, with Cin=7 pF and a shaping time of 50 ns maximum voltage of 235 mV and a rms noise of 3 mV are obtained. Therefore the number of injected electrons is:

$$N°e^{-}injected = \frac{1.25mV * 7\,pF}{1.6 * 10^{-19}\,C} = 54687e^{-} \qquad (3.\ 4)$$

and the ENC:

$$ENC = \frac{Vn}{Vout} * \left(N°e^{-}injected\right) = 698e^{-} \qquad (3.\ 5)$$

To conclude the noise measurements, the preamplifier rms noise is measured varying Cin and Cf. Figure 3.34 illustrates the results. On the first panel the rms noise is plotted versus the Cin value showing for small Cin that the rms noise is smaller with a difference between Cin=1 pF and Cin=7 pF of 0.4 mV. On the second panel is plotted the rms noise versus Cf showing that the rms value increases for smaller Cf and the difference between the smaller Cf value and the bigger Cf value is about 5 mV.

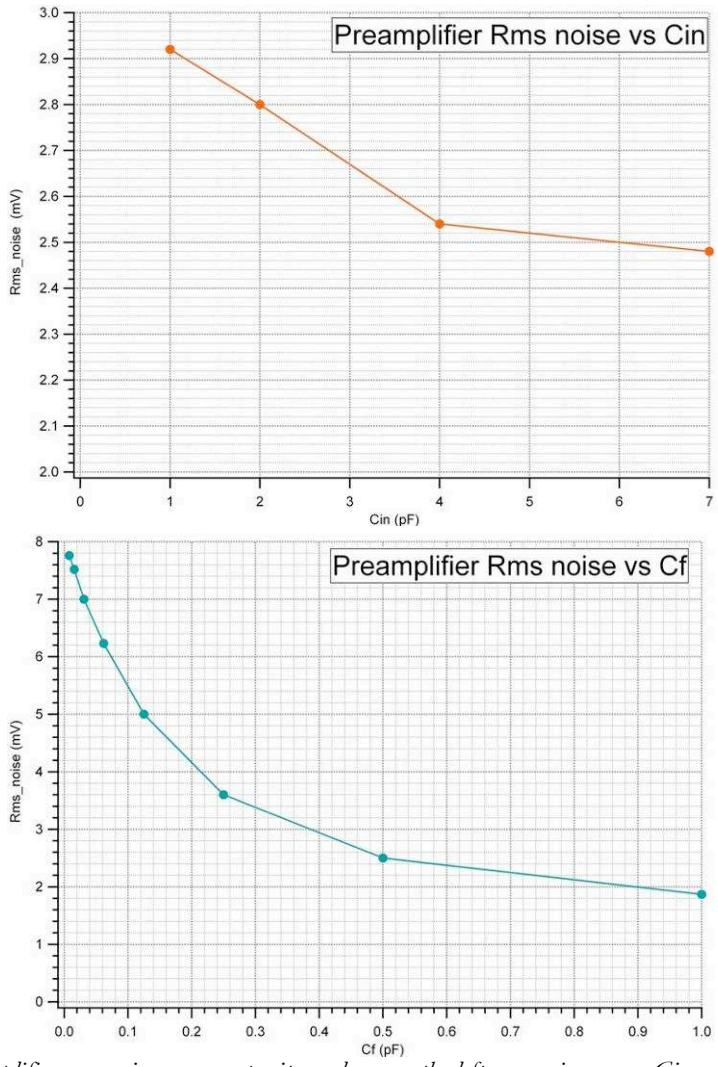

Figure 3.34. Preamplifier rms noise versus capacitor values; on the left rms noise versus Cin and on the right rms noise versus Cf.

4.1. Clock noise

The observations on the oscilloscope of analog signals have demonstrated that a periodical signal overlaps the original one: the clock coupling signal can be one of the causes of the extra noise measured on the ASIC (compared with simulations).
Enabling the clock by Labview (Figure 3.4) is observed that:

- The rms noise values increase with the clock frequency;
- The clock noise is progressively smaller from channel 1 to channel 16;
- The clock noise depends on the preamplifier gain. It decreases with smaller gain.

In Table 3.12 are listed the noise measurements with and without the internal clock. The readout clock (10 MHz) increases the noise of all the analog parts and in particular the fast shaper noise. The 40 MHz noise contribution is so small that it can be considered negligible. A capacitor of 220 μF is placed between the VDD and the ground in order to filter the noise injected by the power supply.

	Rms noise Preamplifier mV	**Max voltage preamplifier mV**	**Rms noise Slow shaper mV**	**Max voltage Slow shaper mV**	**Rms noise fast shaper mV**	**Max voltage fast shaper mV**
Without clock	0.995	85.6	2.2	207	2.5	360
With clock 10 MHz	1.68	86	2.9	211	14	360

Table 3.12. Analog cell noise with and without the 10 MHz internal clock, 10 p.e. at input and preamplifier gain 14.

In order to study how the clock noise modifies the rms values; an external variable clock is used as readout clock. Changing the external clock frequency from 1 MHz to 20 MHz the preamplifier, slow shaper and fast shaper noise are measured and listed in Table 3.13. The results show that the noise increases with the clock frequency.

Variable External clock	**Rms noise Preamplifier mV**	**Max voltage preamplifier mV**	**Rms noise Slow shaper mV**	**Max voltage Slow shaper mV**	**Rms noise fast shaper mV**	**Max voltage fast shaper mV**
1MHz	1.13	85.5	2.5	211	4.3	350
5MHz	1.68	84.8	2.68	210	8	350
10MHz	1.8	87	3	219	13	362
15MHz	2.14	87.5	3.17	216	8.7	361
20MHz	2	88	2.9	213	8.8	360

Table 3.13. Analog cell noise with an external variable clock, 10 p.e. in input and preamplifier gain 14.

4.2. Noise measurements conclusions

The noise measurements have brought to conclude that the ASIC PARISROC has:

- An extra noise in all the analog blocks compared to the simulation results;
- A small quantity of noise that is introduced by the USB cable;
- Rms noise which depends on Cf and less on Cin;
- The parallel noise which depends on Cin and the series noise which is independent on Cin (theoretically this dependence is inverted). Then an extra parallel noise which is introduced by Cin (in particular by the VDD supply);
- An internal shaper noisier than the external one;
- A clock noise that increases the analog blocks rms values; this clock noise depends on the preamplifier gain, is not uniform in all the channels and is injected by the supply connected to the Cin switches.

5. DAC linearity

As explained in § 4.3 Chapter II the two 10-bit DAC fix the discriminators thresholds that form the output trigger. The DAC performances have been checked by the measurement of its linearity. The third tab of the Labview program (Figure 3.5) has been used. It consists in measuring the DAC voltage (Vdac) amplitude obtained for different DAC register values. The data of the two 10-bit DACs linearity, saved by Labview in an Excel file, are then studied to calculate the fit and its residuals. Figure 3.35 gives the evolution of Vdac as a function of the register for the two DACs. The residuals (Figure 3.36) obtained are: from -0.33 to 0.23% for DAC1 and from -0.44 to 0.43 % for the DAC2, showing a good linearity for both DACs.
The first (second) 10-bit DAC has a maximum voltage value of 2.268 V (2.264V) and a minimum voltage of 0.511 V (0.433V) then a LSB of 1.72mV (1.79 mV).

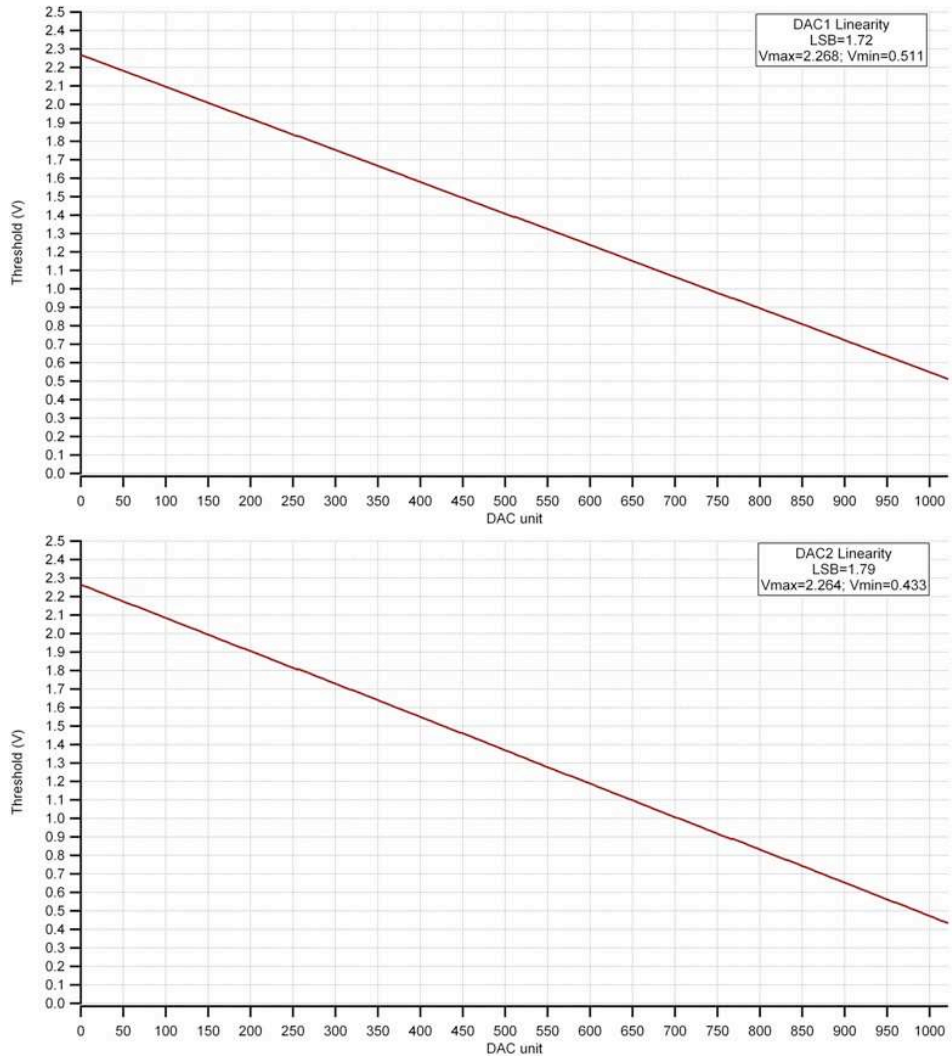

Figure 3.35. Top panel 10-bit DAC1 linearity; bottom panel 10-bit DAC1 linearity.

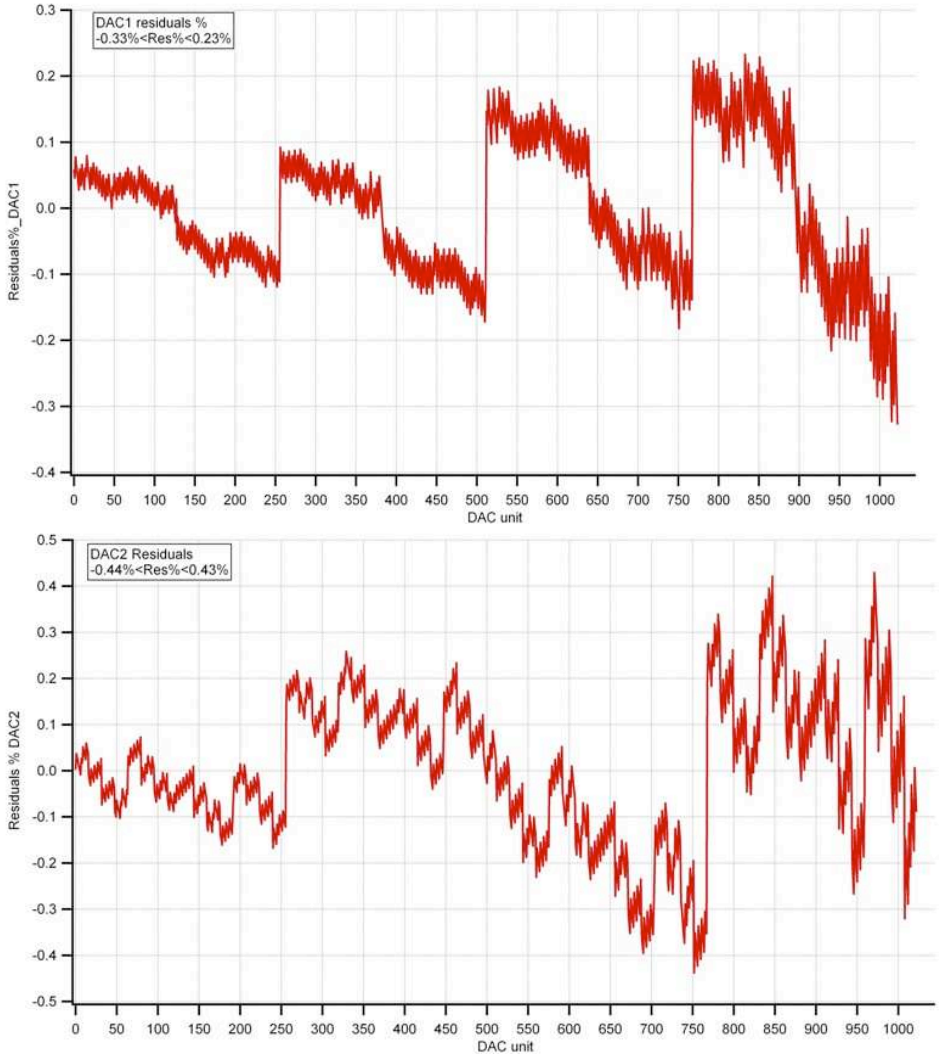

Figure 3.36. The top panels show the DAC1 linearity residuals in % and the bottom panels the respective DA2 linearity residuals in %.

6. Trigger efficiency

The S-curve[52] test is made fixing the injected charge (at a fixed frequency) and changing the threshold level on the discriminator. As the fast shaper is a negative pulse, the discriminator gives an output trigger (top panel on Figure 3.38) when the fast shaper signal goes below the threshold. Several acquisitions (standard is 200) are performed for each DAC value. The resulting trigger efficiency is represented as a function of the threshold. When the signal is lower than the threshold the trigger efficiency is of 100%, when the signal amplitude becomes higher than the threshold, the trigger efficiency falls progressively to zero. The S-Curve test allows study of the trigger efficiency and its dispersion with respect to the threshold can be ascribed to the dispersion of the offsets of fast shaper and discriminator or by the variation in gain between the different channels.
The contribution from the offsets can be extracted by recording the S-curves without any signal at the input for each channel. This corresponds to check the fast shaper pedestal value since the channels should start triggering at its level.
Figure 3.37 (on the top) displays the S-Curve pedestal measurements with the 16 curves superimposed. The spread obtained is of one DAC count (LSB DAC = 1.78 mV) so of 0.06 p.e. This result shows a nice pedestal uniformity which demonstrates the excellent offset control obtained with this SiGe bipolar technology.
The bottom plot of Figure 3.37 represents DAC values for which the 50 % trigger efficiency is obtained. This plot indicates the pedestal dispersion among the channels with a mean pedestal value of 205 UDAC ~ 1.919 V.

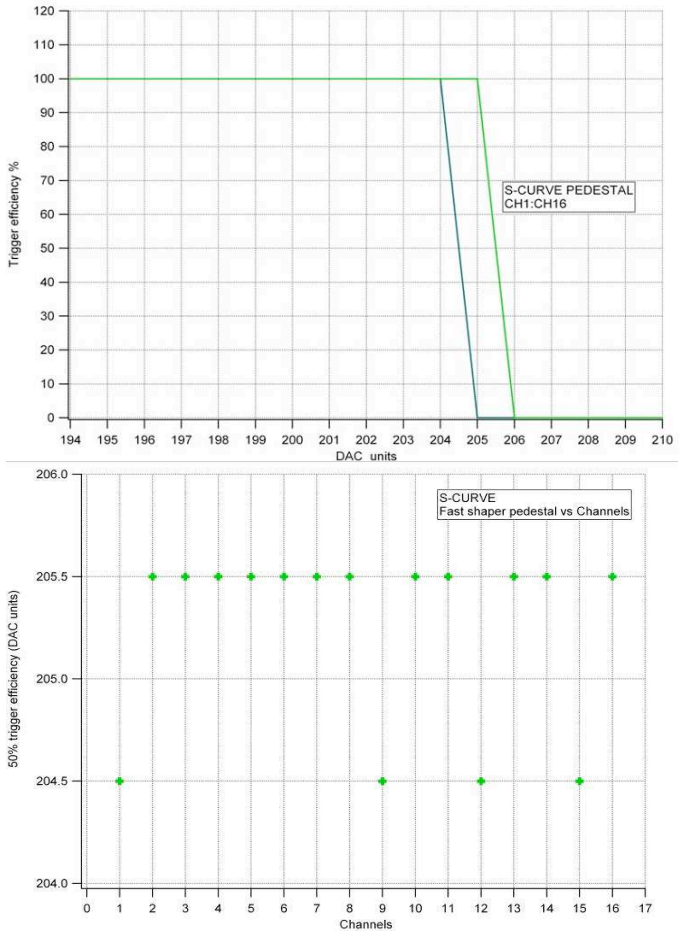

Figure 3.37. Fast shaper pedestal S-Curves for channel 1 to 16 (top). 50% trigger efficiency vs channels (bottom).

[52] The expected S-shape of the curve gives the name of the test. Because of the inverted polarity of the fast shaper signal in this case the shape is inverted.

Each pedestal measurement has a Gaussian distribution:

$$f(x) = \frac{1}{\sigma\sqrt{2\pi}} e^{\frac{-(x-\mu)^2}{2\sigma^2}} \qquad (3.\ 6)$$

The S-Curve function is given by:

$$S-Curve(x) = \int_{-\infty}^{x} f(t)dt = \int_{-\infty}^{x} \frac{1}{\sigma\sqrt{2\pi}} e^{\frac{-(t-\mu)^2}{2\sigma^2}} dt = \frac{1}{2} + \frac{1}{\sigma\sqrt{2\pi}} \int_{0}^{x} e^{\frac{-(t-\mu)^2}{2\sigma^2}} dt = \frac{1}{2} + \frac{1}{2} erf\left(\frac{x}{\sqrt{2}}\right) \qquad (3.\ 7)$$

With $erf(x) = \frac{2}{\sqrt{\pi}} \int_{0}^{x} e^{-u^2} du$ is the Gauss error function.

Inversely, starting with the *S-Curve(x)* function:

$$\left(\frac{d(S-Curve(x))}{dx}\right)_{x=\mu} = \frac{d}{dx}\left(\frac{1}{2} + \frac{1}{\sigma\sqrt{2\pi}} \int_{0}^{x} e^{\frac{-(t-\mu)^2}{2\sigma^2}} dt\right)_{x=\mu} \qquad (3.\ 8)$$

$$\left(\frac{d(S-Curve(x))}{dx}\right)_{x=\mu} = \frac{1}{\sigma\sqrt{2\pi}} \qquad (3.\ 9)$$

Consequently the σ value is:

$$\sigma = \frac{1}{\sqrt{2\pi}\left(\frac{d(S-Curve(x))}{dx}\right)_{x=\mu}} \qquad (3.\ 10)$$

Therefore from the S-Curve slope we can extract the noise value of the fast shaper.

The threshold dispersion was then measured for a fixed injected charge 10 p.e. On Figure 3.38 are represented from top to bottom: the fast shaper and trigger output signals for an input of 10 p.e.; the S-curves obtained with 200 measurements of the trigger for all channels varying the threshold and the 50 % trigger efficiency threshold expressed in number of p.e. for the 16 channel that can indicate the variation in gain between the different channels. The good homogeneity is proved by a spread of 7 DAC units (0.8 p.e.) among the channels.

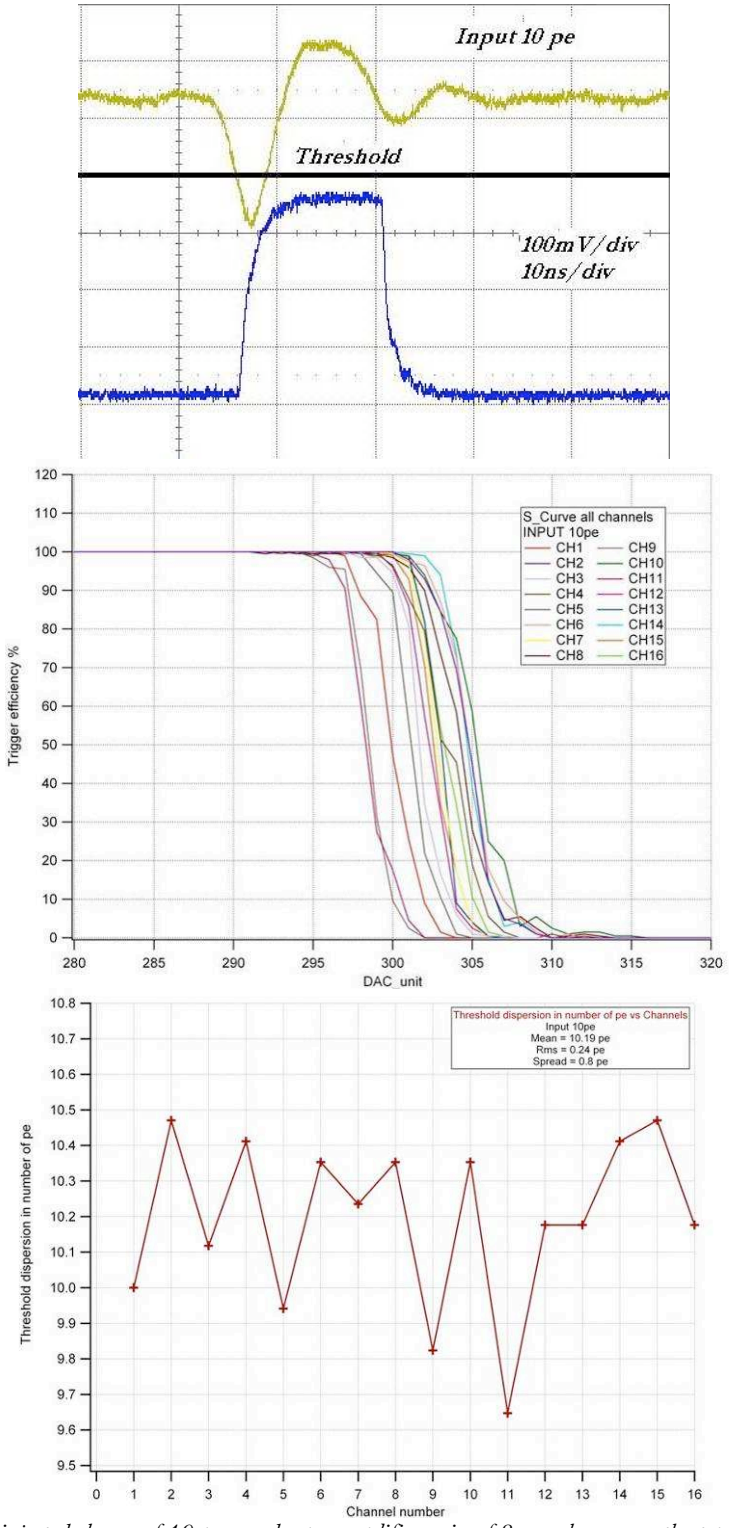

Figure 3.38. For an injected charge of 10 p.e. and a preamplifier gain of 8 are shown: on the top plot the fast shaper and trigger output signals; on the medium plot the S-Curves for all the 16 channels; on the bottom plot the 50 % trigger efficiency values converted in number of p.e. versus the 16 channels.

The trigger efficiency was also studied by scanning the threshold for a fixed channel and changing the injected charge[53]. The top plot of Figure 3.39 shows the trigger efficiency versus the threshold (in DAC units) for the different injected charges, from 0 p.e. (the pedestal = 217 UDAC) to 300 p.e., while the bottom one displays the same measurement until 3 p.e. (480 fC).
The 50% trigger efficiency values extracted from the last measurement are plotted, in mV, versus the injected charge (Figure 3.40). The linearity is correct down to 100 fC which corresponds to 10 σ (σ =13 fC) noise instead of the 5 σ noise expected from theory. The reason of this result which doesn't match the project requirement to put the threshold at 1/3 of p.e. (~ 50 fC) will be given in the next section.

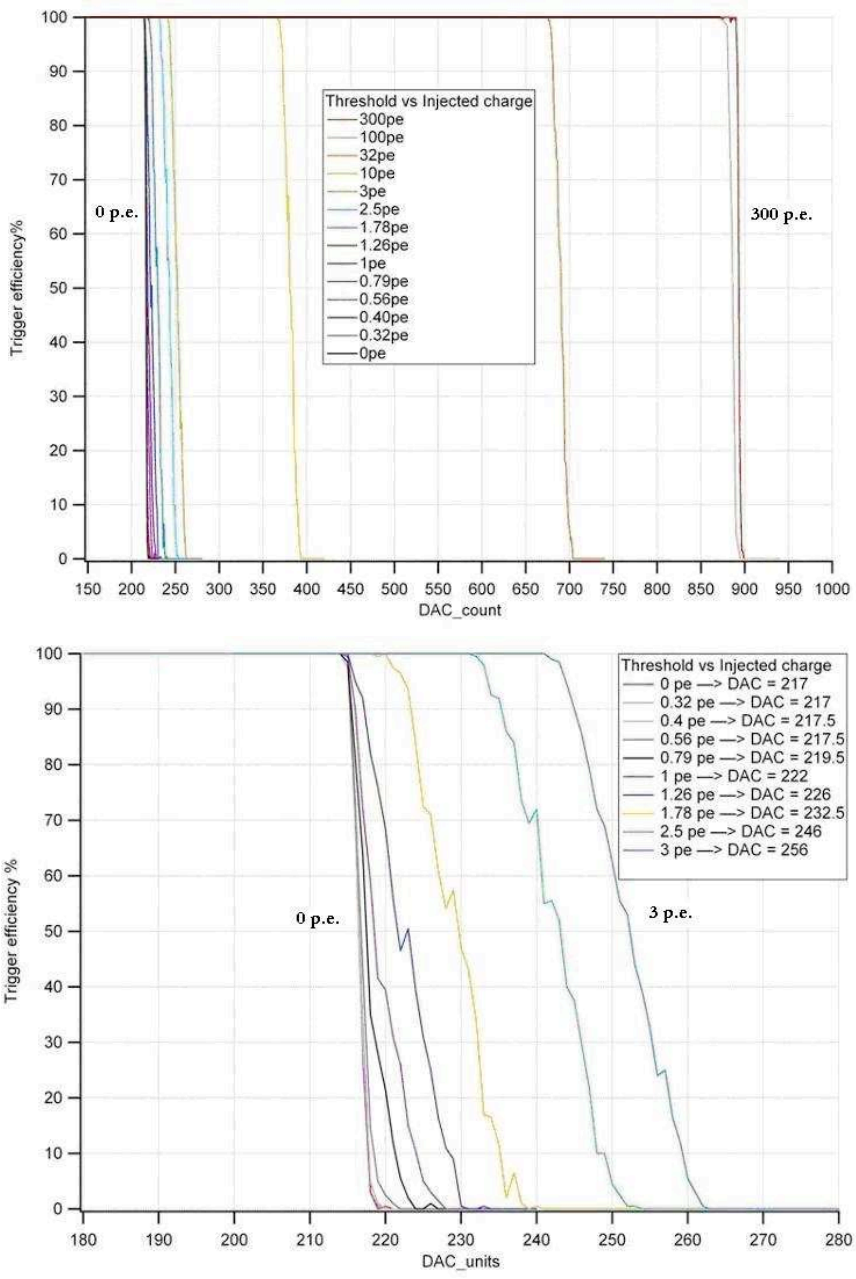

Figure 3.39. Trigger efficiency vs DAC count until 300 pe (left) and until 3 pe (right).

[53] The tests described until now have been done on a chip numbered as "chip 2". The chip used in next tests will be the chip numbered "chip 6". For some specific investigations the output NOR16 of chip 2 has been disabled becoming inusable for the next S-Curve tests.

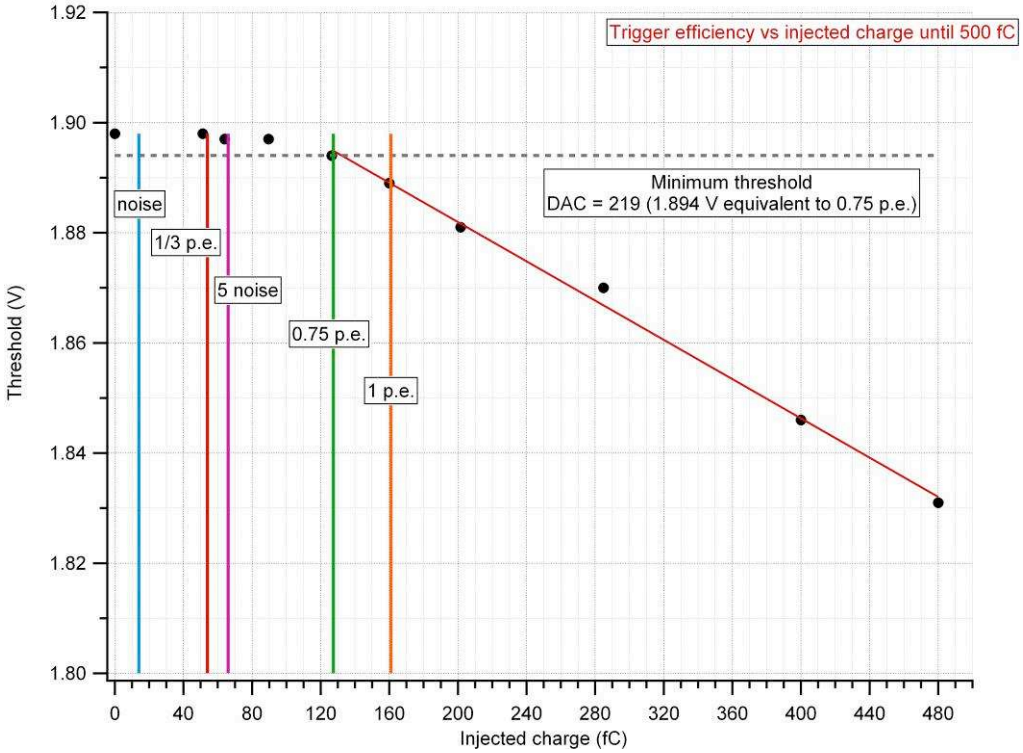

Figure 3.40. Threshold vs injected charge until 500 fC.

6.1. Discriminator Coupling

The discriminator output trigger obtained when the threshold is lower than the fast shaper signal have been observed on the oscilloscope thanks to the digital test pins located on the test board (Figure 3.2). Same extra output triggers have been noticed and a peculiar investigation has been done. This behavior has been attributed to a coupling signal among the channels that has been confirmed with measurements.

Fast shaper output signal is observed for channel 2 while injecting a 10 p.e. signal in channel 1. Figure 3.41 shows in yellow the discriminator output trigger detected on channel 1 and in blue the coupling signal on channel 2. The preamplifier input capacitance is set at Cin 4 pF (Gain 8) and the DAC threshold at 250 UDAC.

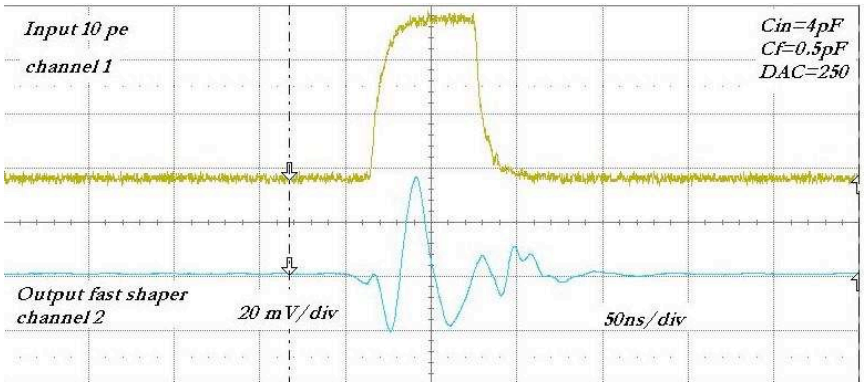

Figure 3.41. Channel one output trigger (yellow) and channel two coupling signal (blue).Cin = 4pF.

To interpret this signal, tests with different chip parameters have been performed changing the preamplifier gain. The coupling signals observed with different Cin values indicates an important dependence.

Indeed Figure 3.42 shows the coupling signal for a preamplifier gain 14 (Cin 7pF) with a coupling signal smaller than for a gain of 8 (Figure 3.41), this mean that the coupling signal is injected at the level of the input by the VDD of Cin.

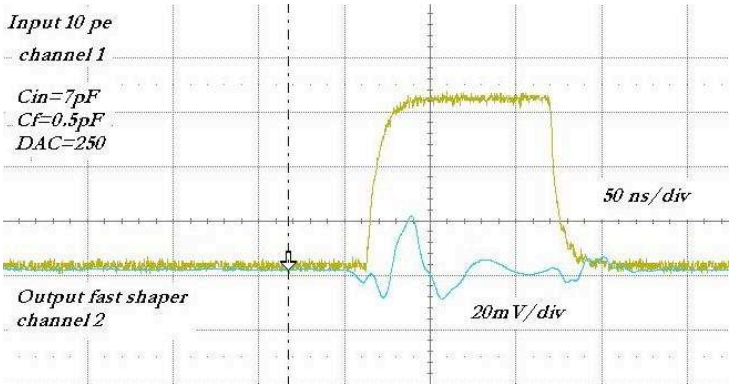

Figure 3.42. Channel one output trigger (yellow) and channel two coupling signal (blue).Cin=7pF.

These coupling signals are observed in all the channels and this extra signal depends on the discriminator output signal as illustrated by the Figure 3.43 and Figure 3.44. For the first one, the trigger polarity has been inverted, by a slow control bit, and an inverted coupling signal has been observed on channel 2. For the second one the high level voltage VH (of the trigger output buffer) is changed from 3.3 V to 1.5 V inducing a coupling signal with smaller amplitude.

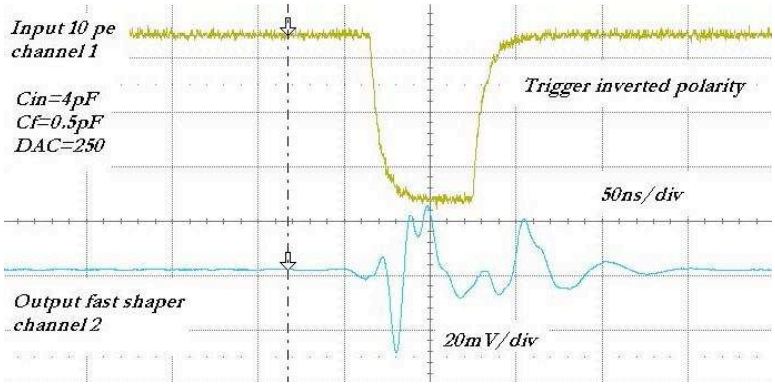

Figure 3.43. Channel one output trigger inverted (yellow) and channel two coupling signal (blue).Cin= 4pF.

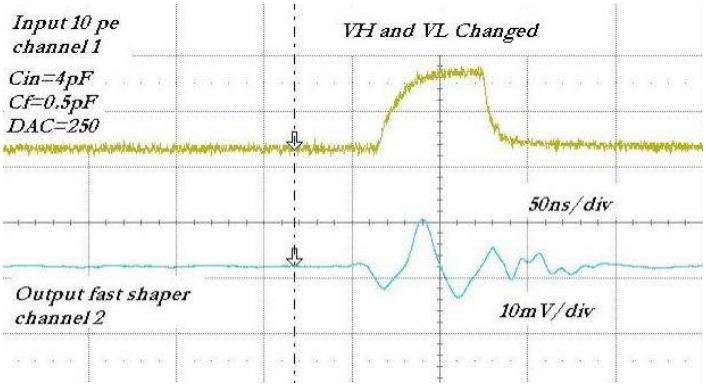

Figure 3.44. Channel one output trigger (yellow) with VH=1.5V and channel two coupling signal (blue).Cin= 4pF.

The investigation on the coupling signals has been done, also, with the S-Curve test. Figure 3.45 shows the S-curve for the 16 channels obtained injecting a high input signal of 300 p.e. in channel one with a preamplifier gain 8. These curves are plotted after pedestal subtraction (mean value for the 16 channels 205 UDAC); the red curve represents the trigger efficiency for the channel two and the other curves, shifted with respect to the red one, are the measurements done for channel 3 to 16.

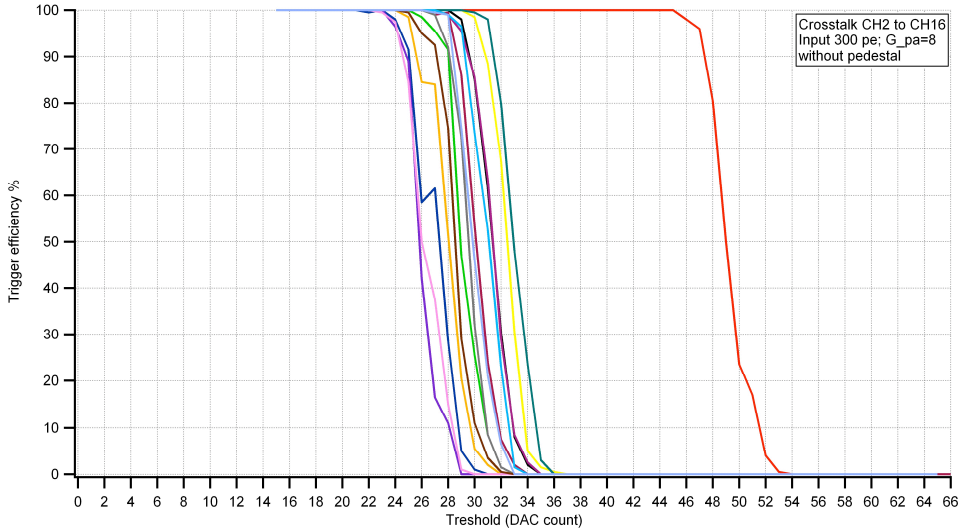

Figure 3.45. S-curve for channel 2 to channel 16 with an input signal of 300 p.e. in channel one and preamplifier gain 8.

From this plot are extracted the 50 % trigger efficiency values from channel 2 to 16 and the distribution is displayed on Figure 3.46. The mean value is 31 UDAC and the rms value 5 UDAC.
These values are then compared with the one of channel 1 (664 UDAC) using the following formula and the coupling signals obtained in % are illustrated on Figure 3.47.

$$Coupling\_signal\_\% = \frac{50\%\_Trig\_eff\_CHi}{50\%\_Trig\_eff\_CH1} \times 100 \qquad (3.\ 11)$$

The statistical calculations give a minimum value of 4 %, a maximum of 7.5% and a mean of 4.7%. These values and the plot on Figure 3.47 indicate that the coupling signal has the same amplitude in all the channels. This demonstrates that this extra signal is a coupling signal and not a crosstalk signal. This last is a signal that is induced in close channels and is caused by capacitive coupling in the circuit substrate. The crosstalk signal has amplitude that decreases in channels distant from the one where the signal has been injected.

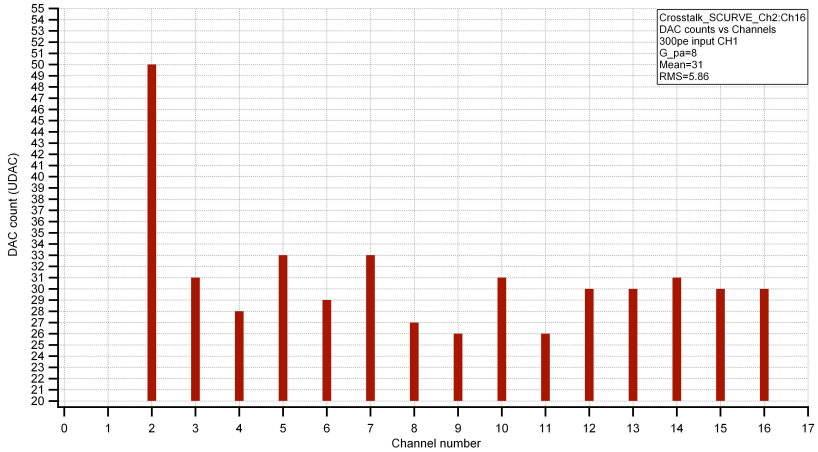

Figure 3. 46. 50% trigger efficiency (UDAC) versus channels from channel two to channel 16.

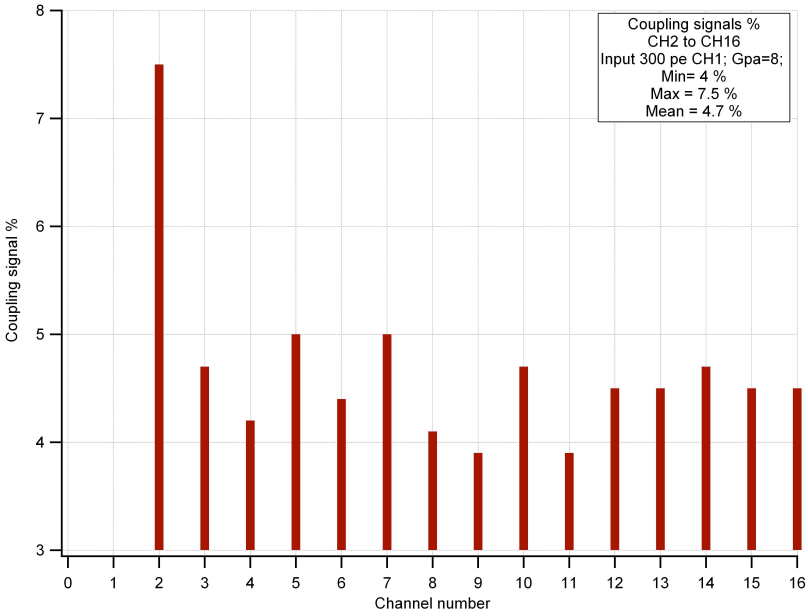

Figure 3.47. Coupling signal in % versus channels (from channel two to channel 16).

6.2. S-Curve test for different ASICs

Five different chips have been characterized to compare their performances, in particular in terms of clock noise. These chips have been tested with different configurations as various preamplifier input capacitor values and clocks.

Figure 3.48 and Figure 3.49 display the S-curves versus the DAC counts obtained, while no signal is injected, for the channel one (top plots) and the 16 channels (bottom plots) respectively without and with 10 MHz clock and setting Cin to a value of 4 pF.

The comparison between the two measurements indicates that the presence of the 10 MHz clock shifts the S-Curves therefore the pedestal level of the channel one from 209 UDAC to 218 UDAC then of 9 UDAC. Moreover measurements performed for all channels give a larger spread among them from 4 UDAC without clock to 5 UDAC with the clock.

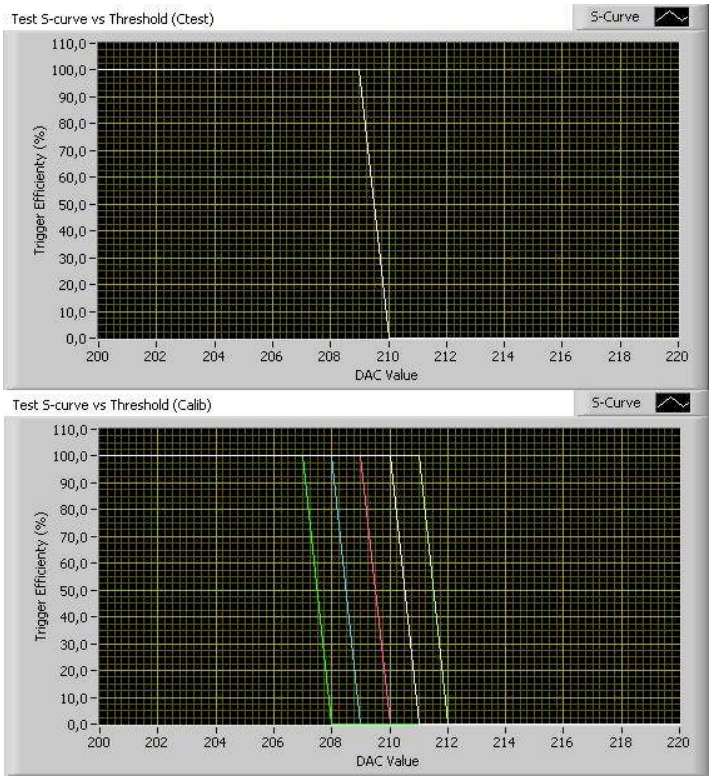

Figure 3.48. S-Curve for chip 6. On the top panel the S-curve for Ch1 and on the bottom for all channel with 4 pF set on the preamplifier input and without clock.

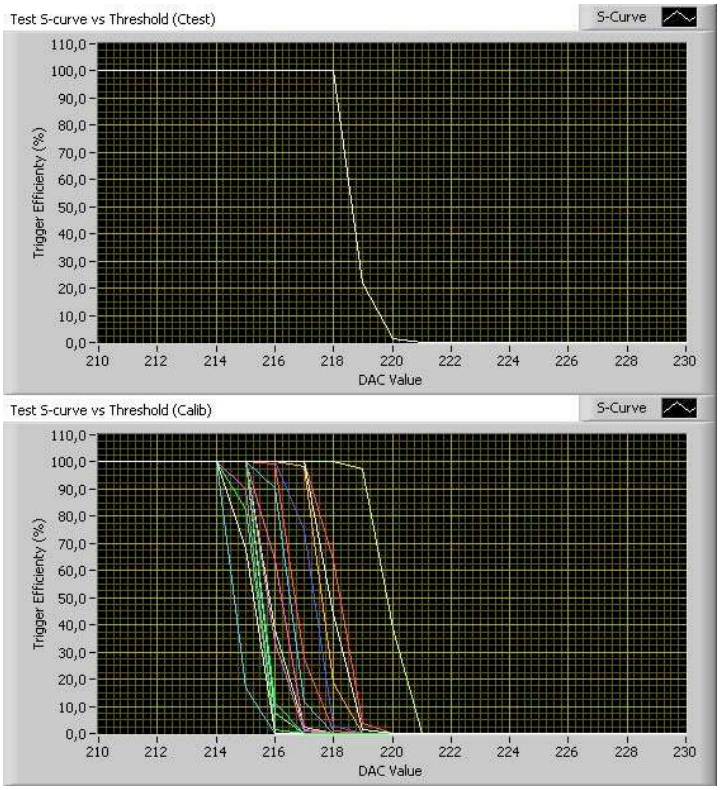

Figure 3.49. S-Curve for chip 6.On the top picture the s-curve for Ch1 and on the bottom for all channel with 4 pF set on the preamplifier input and with clock.

Such measurements have a direct link to the fast shaper pedestal since the trigger efficiency should start dropping from 100 to 0 % for DAC values close to the pedestal level.
The five chips have also been tested with Cin 7pF. The 50 % trigger efficiency values of the five chips are listed on Table 3.14 and Table 3.15 that indicate the measurements respectively with and without the 10 MHz clock for the two different Cin values. It can be deduced that the pedestal level is dependent from the Cin value if the 10 MHz clock is on.

	Pedestal (UDAC)	
	Cin = 4pF	**Cin = 7pF**
Chip6	218.5	214
Chip7	206.7	201.5
Chip8	217.5	213.5
Chip9	226	222.5
Chip10	219.5	214

Table 3.14. With Clock

	Pedestal (UDAC)	
	Cin = 4pF	**Cin = 7pF**
Chip6	209	209
Chip7	196.5	196.5
Chip8	208.5	208.5
Chip9	216.5	216.5
Chip10	209.5	209.5

Table 3.15. Without clock

These results are illustrated by the Figure 3.50 which represents the pedestal value as a function of the chip number with the 10 MHz clock for Cin 4 pF (blue curve) and for Cin 7 pF. (green curve). In Figure 3.51 are calculated and plotted the differences between the two measurements. Setting Cin to 4 pF, the pedestal values are higher by 3.5 UDAC to 5.5 UDAC.

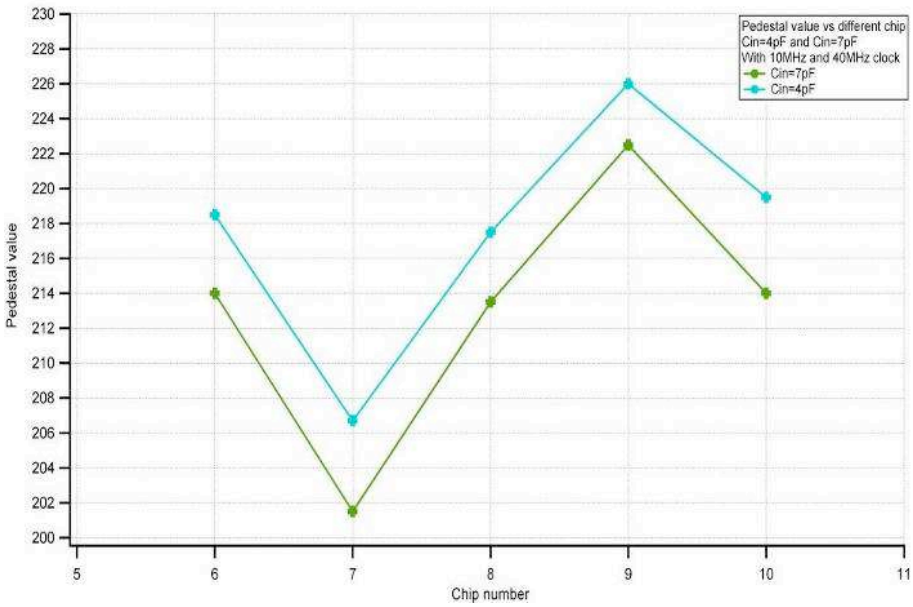

Figure 3.50. Pedestal value for chip 6 to 10 with clock and different Cin. Blue curve Cin= 4 pF. Green curve Cin= 7 pF

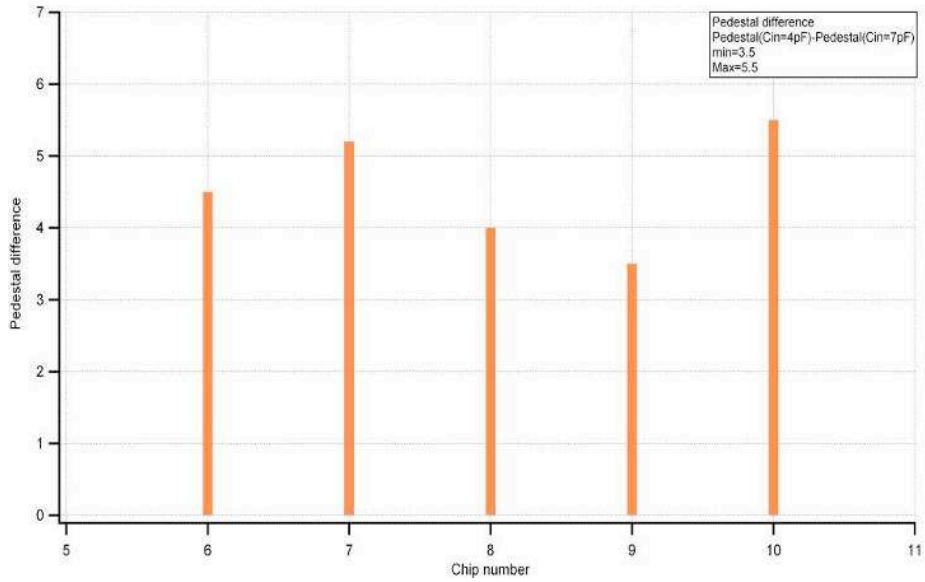

Figure 3.51. Pedestal differences between Cin= 4pF and Cin= 7pF with clock.

On Figure 3.52 are plotted the pedestal values without clock for the five chips: the pedestal has a minimum value of 196.5 and a maximum value of 216.5 so a spread of 20 UDAC.

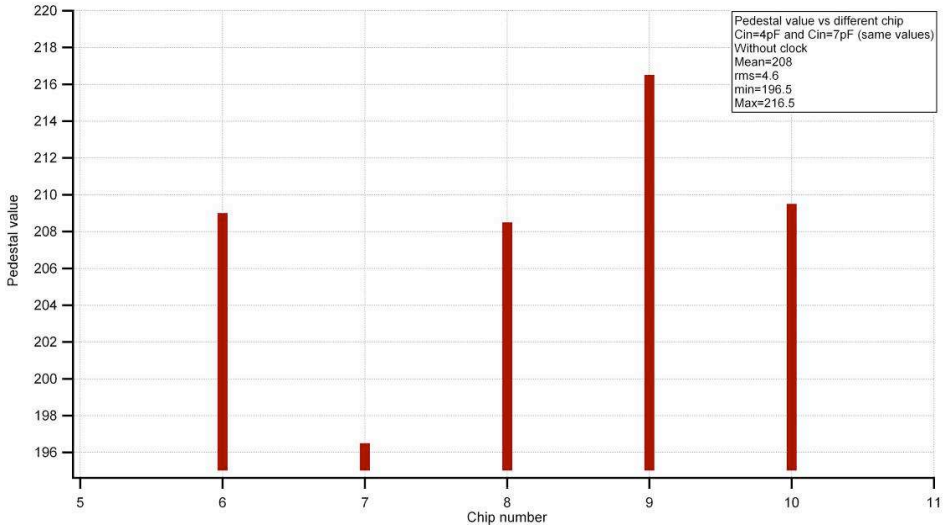

Figure 3.52. Pedestal distribution of the five chips without clocks. Pedestal in UDAC versus chip number.

6.3. S-Curve measurements conclusions

The S-Curve tests brought to important conclusions:

- The pedestal dispersion among channels of 0.06 pe, demonstrates good pedestal uniformity and so a good offset control obtained with the SiGe bipolar technology.
- The spread of 0.8 p.e. among channels, injecting an input charge, indicates a good homogeneity of the chip. A large spread can indicate a variation in gain among the channels.
- The trigger sensitivity study shows that the threshold is limited to 10 σ noise, instead of the theoretical 5 σ noise. The project requirement to set the threshold at 1/3 of p.e. is not satisfied because of the coupling signal.

- A discriminator coupling signal is observed: it changes with Cin value and so is injected by the supply VDD.
- A statistic among chips gives poor pedestal uniformity and confirms the clock noise.

7. ADC measurements

The analog-to-digital converter is an essential block in the ASIC; it forms the critical link between the analog front-end and back-end digital computers that must treat the data then various tests have been done to check its performances and to characterize the whole chain.
The ADC conversion is made (as explained in § 4.6 Chapter II) by the ADC discriminator comparing a ramp with the charge or time values saved in the analog memory.

7.1. ADC performances

As explained in the introduction an external ADC input (Figure 3.53) is added in the chip design (common for all channels) with the purpose to test the ADC performances. The standard ADC input or the external input can be chosen with a slow control parameter (Choice in ADC Figure 3.3).

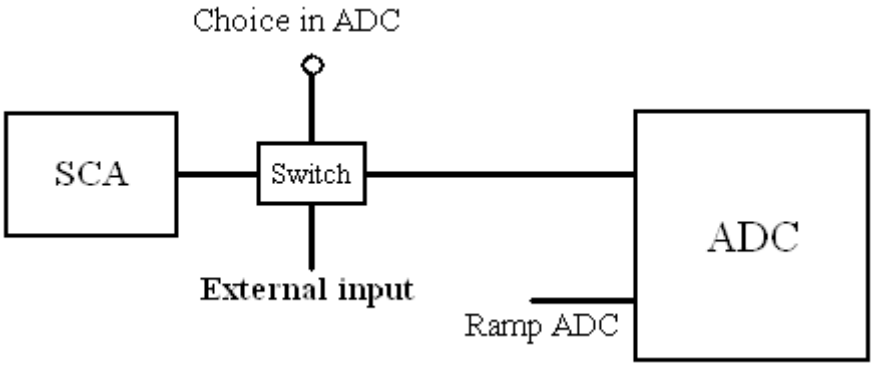

Figure 3.53. Input ADC general schematic.

A DC voltage is injected from the internal DAC to the external input of the ADC and the ADC values for all the channels are measured.
With a DAC value of 500 (1.450 V) at the 12-bit ADC (LSB=270 μV) input, the measurement is repeated 10000 times for each channel. Figure 3.54 shows the results obtained on the first panel of the Labview program. The first plot (top left panel) represents the minimal, maximal and mean values and overall acquisitions for each channel.
In the second plot (bottom left panel) there are the rms charge values versus channel number with spreads less than one ADC unit (UADC). Finally the third plot (right panel) shows an example of charge amplitude distribution for a single channel; a central value of 1961 UADC with a spread of 5 UADC is obtained.

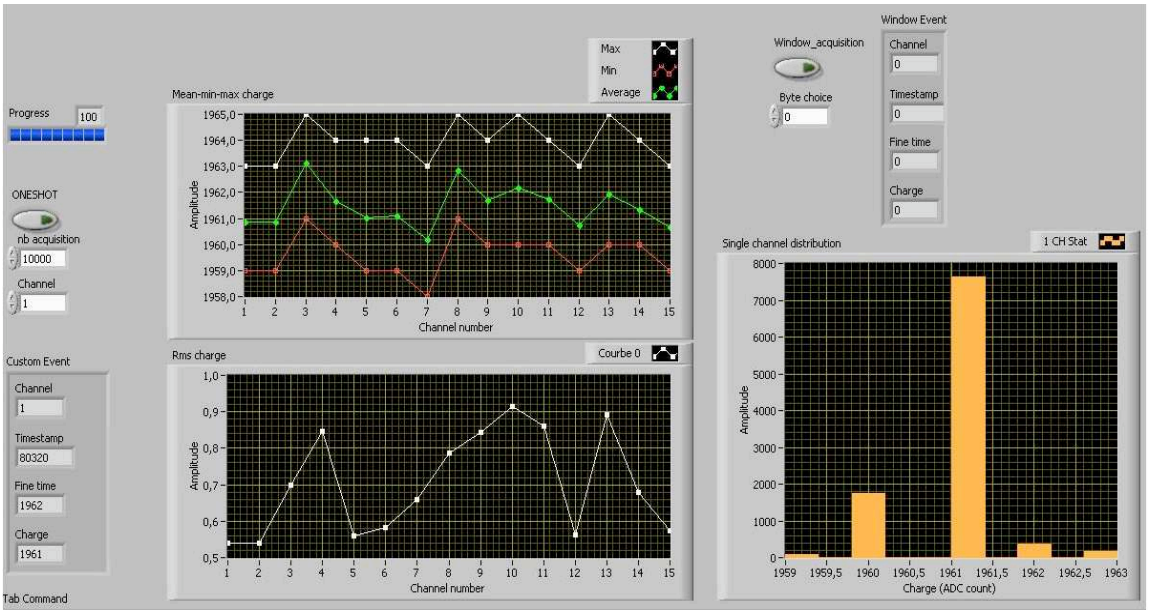

Figure 3.54. ADC performance with an external input voltage. Channels uniformity (top left), rms values for all channels (bottom left) and single channel distribution (right) are represented.

The DC voltage reference of the ADC ramp is 928 mV. In Figure 3.55 is displayed the picture of the 12-bit ramp captured on the oscilloscope. Whit an ADC value measured of 1961 UADC that corresponds to 527 mV (1061 * 270 µV), adding the ramp reference level of 928 mV, the voltage level measured is of 1.455 V that corresponds to the voltage level injected.

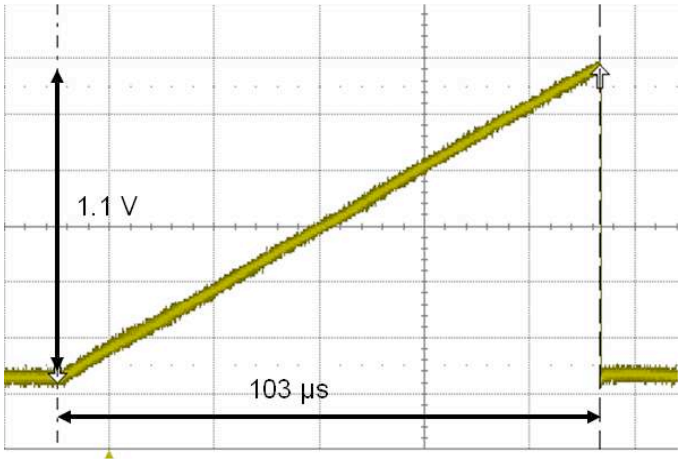

Figure 3.55. 12-bit ADC ramp.

On Figure 3.56 and Figure 3.57 are displayed the other two ADC ramps observed on the oscilloscope: on the top the 10-bit ramp and on the bottom the 8-bit ramp.

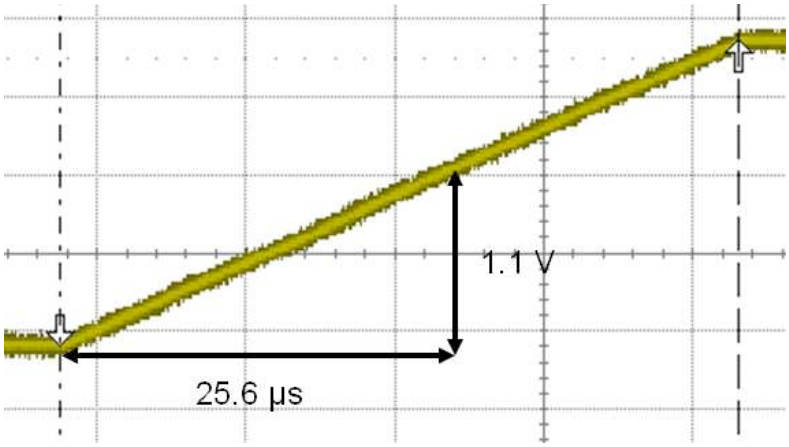

Figure 3.56. 10-bit ADC ramp.

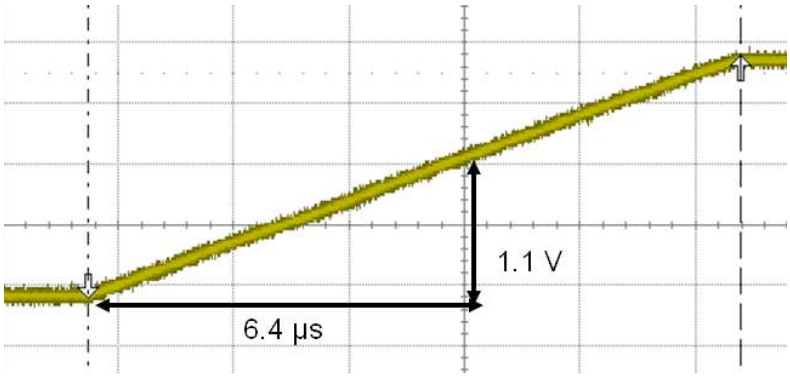

Figure 3.57. 8-bit ADC ramp.

The ADC is suited to a multichannel conversion so the uniformity and linearity are studied in order to characterize the ADC performances. On Figure 3.58 is represented the ADC transfer function for the 10-bit ADC versus the input voltage level. All channels are represented and have plots superimposed.

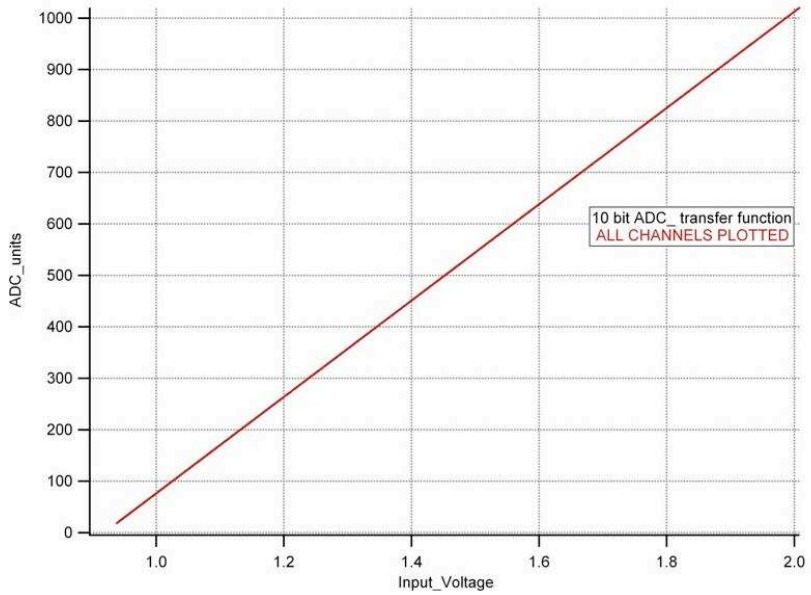

Figure 3.58. ADC transfer function vs input charge. 10-bit ADC. 15 curves superimposed for all channels.

The nice homogeneity observed is confirmed by the linear fit parameters comparison. In Figure 3.59 are plotted the slope and the intercept distributions for all channels; channel 13 is not plotted because of a short circuit in the layout that put the 13th channel to zero in the ADC output. The rms slope value of 0.143 and the rms intercept value of 0.3 confirm good 10-bit ADC uniformity (Table 3.16).

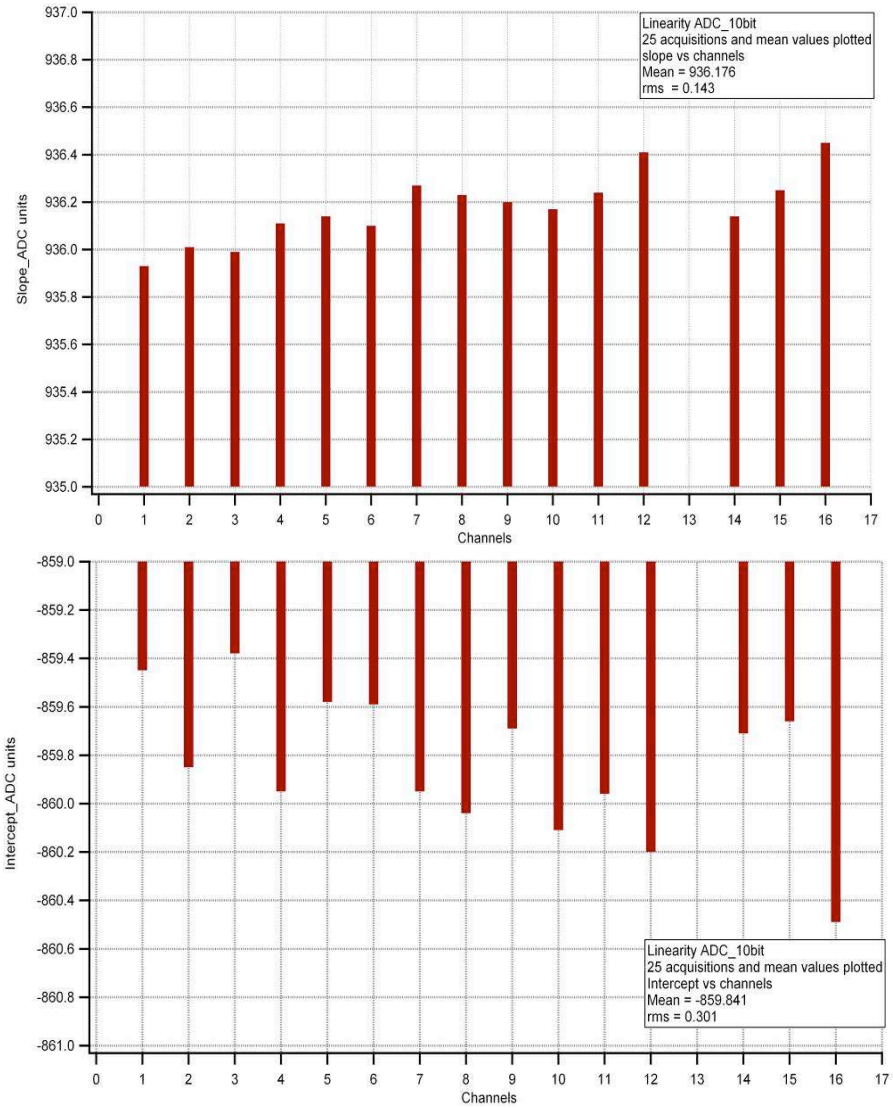

Figure 3.59. Evolution of the fit parameters (slope on the top and intercept on the bottom) as a function of the channel number.

10 bit ADC	Slope	Intercept
Mean	936.17	-859.8
Rms	0.143	0.301

Table 3.16. 10-bit ADC slope and intercept parameters. 25 acquisitions for each channel.

Another good result obtained in measurement is the ADC linearity. In Figure 3.60, 3.61, 3.62 are shown respectively the 12, 10 and 8 bit ADC linearity plots with the 25 measurements made at each input voltage level. The average ADC count values are plotted versus the input signal. The residuals from -1.5 to 0.9 ADC units for the 12-bit ADC; from -0.5 to 0.4 for the 10-bit ADC and from -0.5 to 0.5 for the 8-bit ADC prove the good ADC behavior in terms of integral non linearity (INL). The LSB values calculated for each ADC are: 270 μV for 12-bit ADC; 1 mV for 10 bit ADC and 4.3 mV for 8-bit ADC.

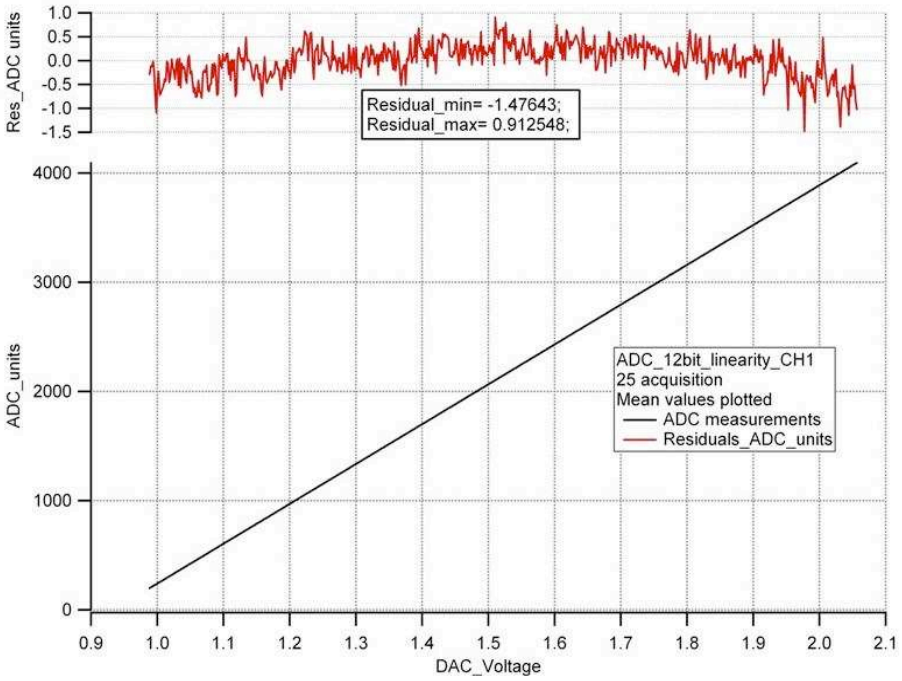

Figure 3.60. 12-bit ADC linearity.

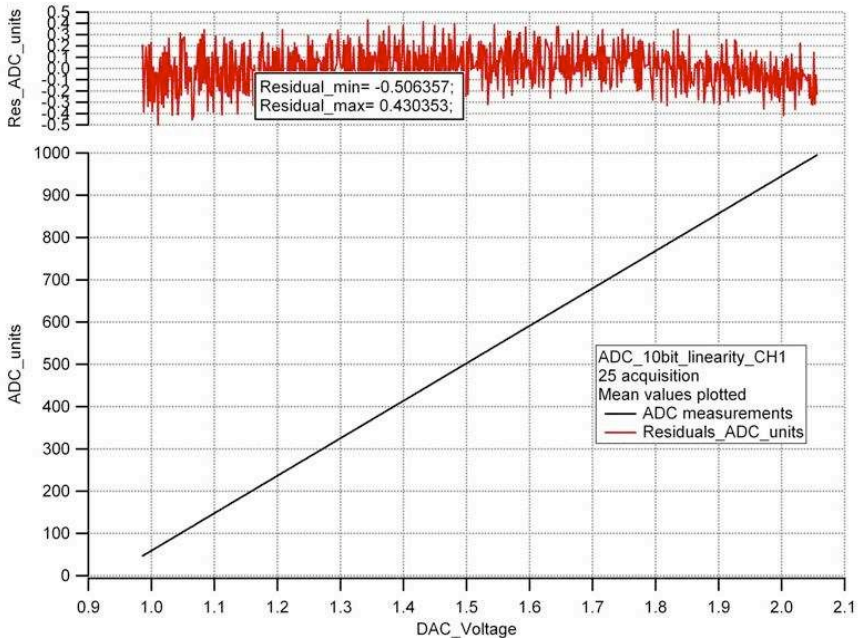

Figure 3.61. 10-bit ADC linearity.

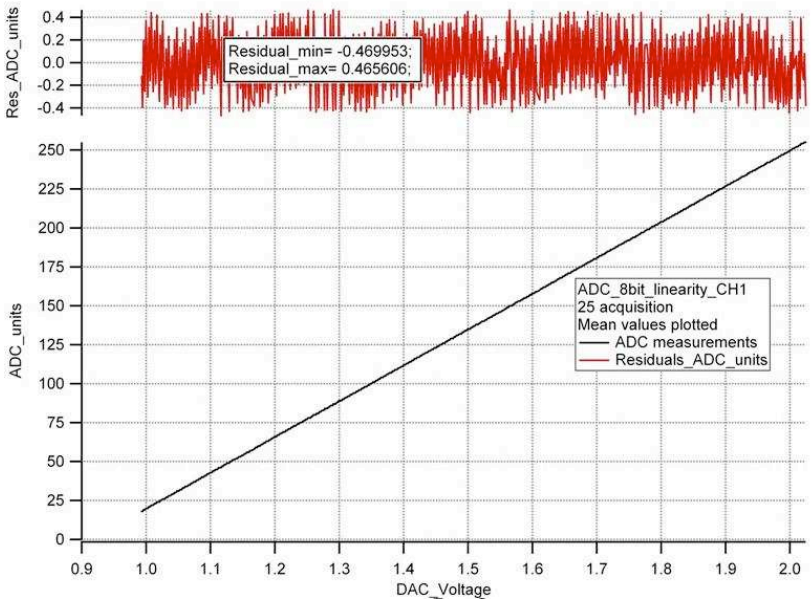

Figure 3.62. 8-bit ADC linearity.

7.2. Charge measurements

A whole test chain has been done checking the converted values of the charge voltage levels stored into the analog memory.
In Figure 3.63 are displayed the signal observed with the oscilloscope to check the T&H performances before the ADC conversion testing.
The yellow curve is the slow shaper signal, the pink curve the T&H signal and the blue one is the slow shaper maximum signal stored in the SCA, this value is then converted by the ADC.

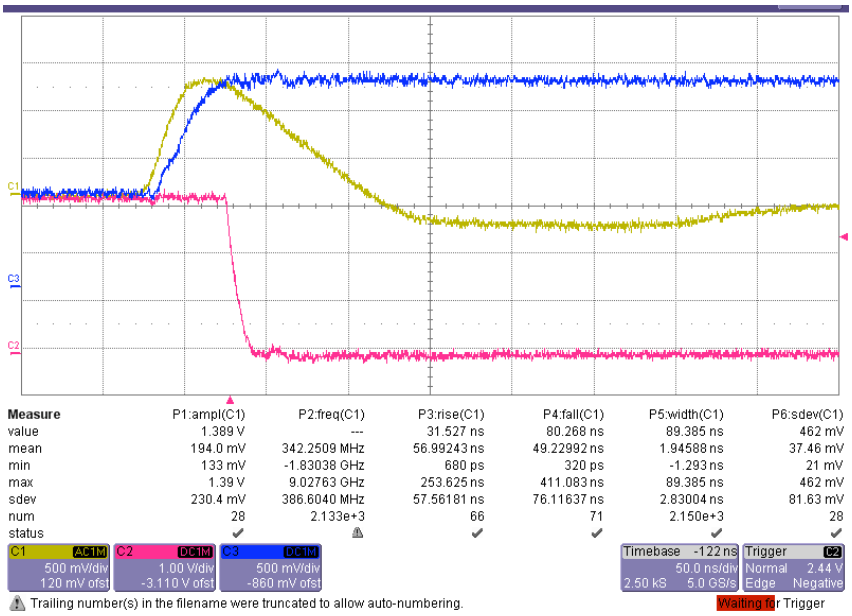

Figure 3.63. Yellow curve: slow shaper signal; pink curve: T&H signal; Blue curve: the slow shaper maximum signal stored in the SCA.

To store exactly the maximum slow shaper voltage, a delay box is conceived in the chip design, to delay the trigger signal and therefore the T&H signal. This delay is tested changing the delay bit by slow control

(Figure 3.3) and measuring the DC voltage levels observed at the output of the SCA (the blue curve on Figure 3.63) then the 50 ns slow shaper output waveform is reconstructed. In Figure 3.64 is represented the plot of the held signal versus the slow control bit number to change the delay.

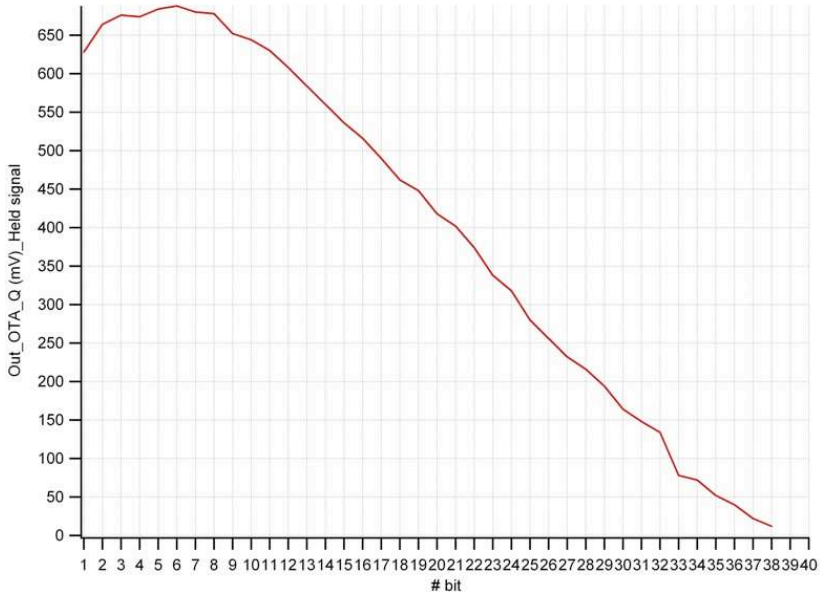

Figure 3.64. Held signal values versus the slow control bit number.

From this figure it is clear that the bit 5 must be on to measure the 50 ns slow shaper maximum.
Before testing the ADC conversion injecting a charge, the slow shaper pedestal is checked with the ADC. On Figure 3.65 are displayed the Labview tabs obtained for the measurements with the three ADC precision (12, 10 and 8 bits).
The chip is in default configuration with preamplifier input capacitor at 4 pF and feedback capacitor at 0.5 pF. 1000 acquisitions are made for each channel. In each tab on the top panel are plotted the maximum, minimum and average values for each channel; on the middle panel the rms values for each channel and on the bottom panel the distribution for one channel (channel 1). The three charge distributions for the channel one have the following values:

- Minimum at 255, maximum at 315 and mean at 280 UADC with noise of 10 UADC (~ 2.7 mV) for the 12-bit ADC;
- Minimum at 63, maximum at 79 and mean at 74 UADC with noise of 2.6 UADC (~ 2.7 mV) for the 10-bit ADC;
- Minimum at 18, maximum at 20 and mean at 19 UADC with noise of 0.58 UADC (~ 2.5 mV) for the 8-bit ADC.

The holes on the channel one distribution for the 8-bit ADC are due to the Labview way of plotting and not to the ADC performance.

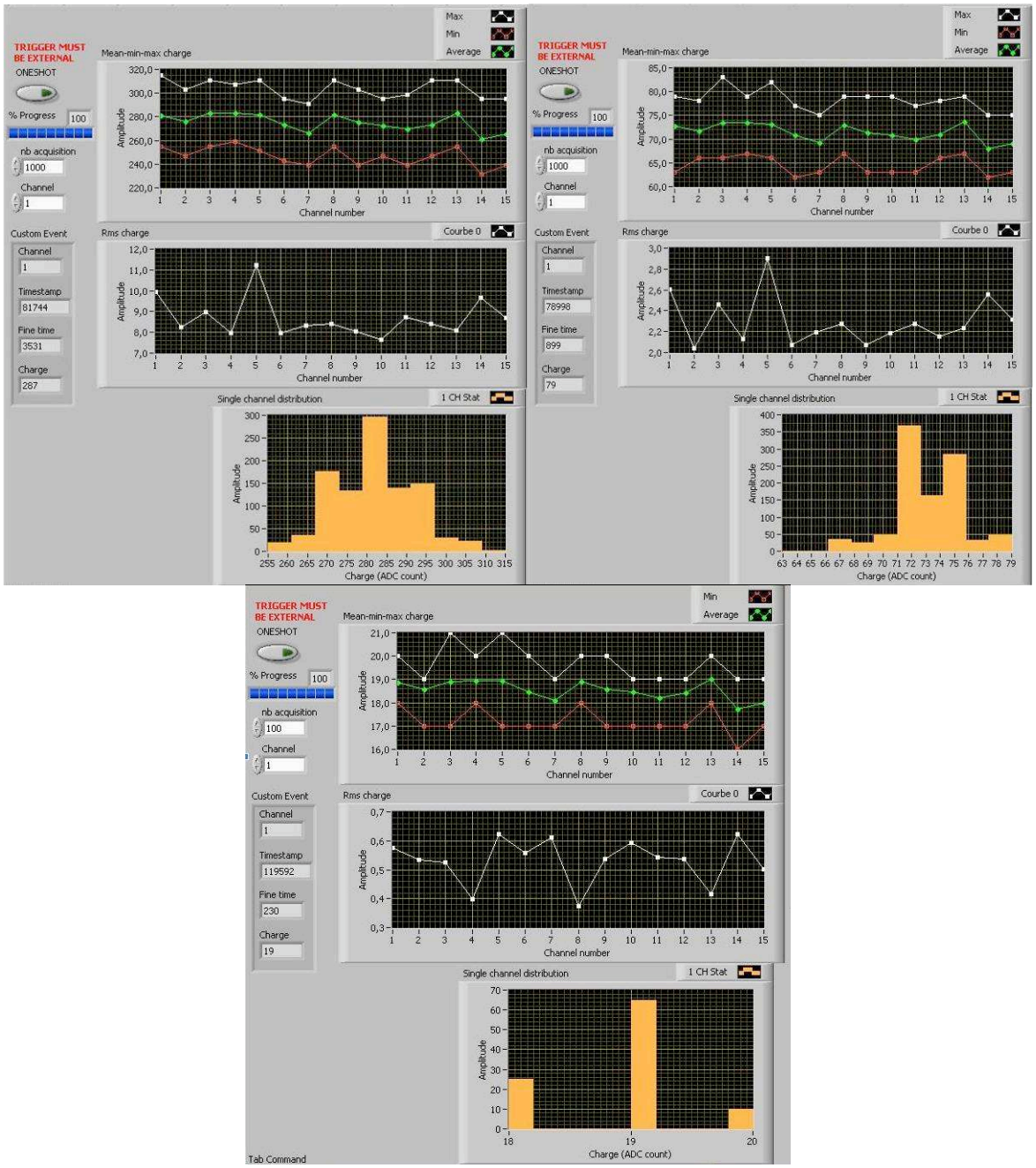

Figure 3.65. ADC pedestal. On the top left pedestal measurement with 12-bit ADC; on the top right pedestal measurement with 10-bit ADC; on the bottom pedestal measurement with 8-bit ADC.

The whole chain is now tested by injecting a charge in the input of the channel: the signal is amplified, auto- triggered, held in the SCA cell and converted by the ADC. The preamplifier gain is set to 14 in order to maximize the signal to noise ratio and the delay cell is set to bit 5 to memorize the maximum slow shaper voltage. With a shaping time of 50 ns, the 10-bit ADC converted data are plotted on left of Figure 3.66 versus the input charge (from 3 to 50 p.e.). The number of events read and converted for each input is around 28000 and the mean value of each conversion is plotted.
A nice linearity of 1.5% and a noise of 6 UADC are obtained (~ 6 mV). In Table 3.17 are listed the setting value for the measurements and the main results.
The right panel of Figure 3.66 displays the charge distribution for the channel one and 3 p.e. of injected charge. The distribution with a hole each two ADC count is due to the clock noise that is overlapped on the signal.

	Min ADC count	Max ADC count	Residuals
10 bit ADC Gpa 14 SSH 50ns LSB 1 mV	132 at 3 p.e.	989 at 50 p.e.	from 6 to 14 UADC

Table 3.17. Setting value for charge measurements and the main results; 10-bit ADC.

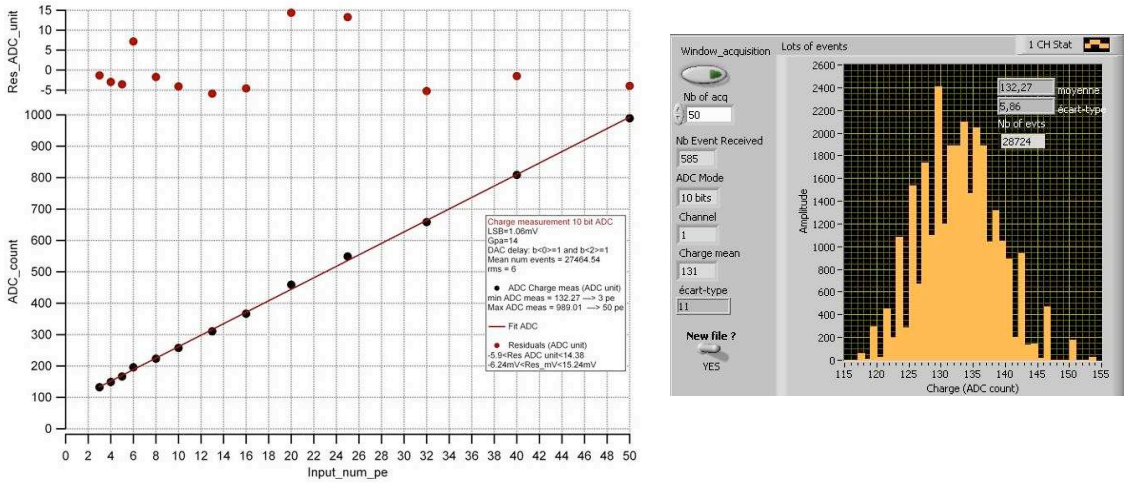

Figure 3.66. Right panel: 10-bit ADC count versus the input charge (from 3 to 50 pe). Left panel: charge distribution for channel one for 3p.e..

The same measurements are repeated for 8 and 12-bit ADC with the same configuration and injected charges. On Figure 3.67 (Left plot) is represented the plot for the 8-bit ADC with linearity at 1.6% and a noise of 1.53 UADC (~ 6mV). In Table 3.18 are listed the setting value and the main results for these measurements. The charge distribution for channel one and 3 p.e. of injected charge is shown on the right plot of Figure 3.67. The hole is not present for the 8-bit ADC because the LSB of this ADC is of 4.3 mV; the steps of conversion are large to detect the clock noise.

	Min ADC count	Max ADC count	Residuals
8 bit ADC Gpa 14 SSH 50ns LSB 4.3 mV	33 at 3 pe	241 at 50pe	from 2 to 3 UADC

Table 3.18. Setting value for charge measurements and the main results; 8-bit ADC.

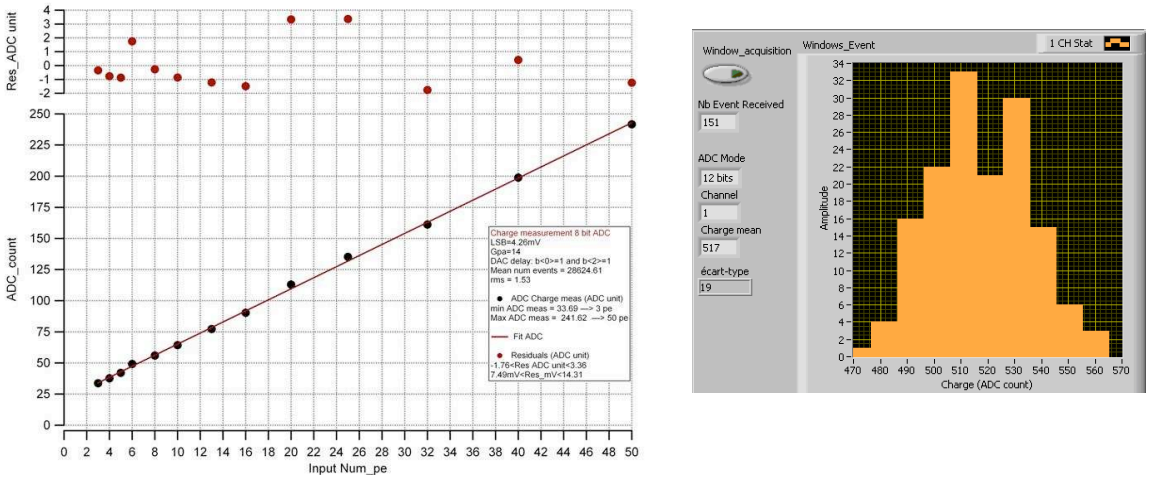

Figure 3.67. Right panel: 8-bit ADC count versus the input charge (from 3 to 50 pe). Left panel: charge distribution for channel one for 3p.e.

Finally on Figure 3.68 is shown the plot for the 12-bit ADC with linearity of 1.5% and a noise of 23.7 UADC (~ 6 mV). In the Table 3.19 are listed the setting value and the main results for these measurements. The charge distribution for 3 p.e. of injected charge is shown on the right of Figure 3.68. The holes are more evident for the 12-bit ADC because of the smaller LSB value.

	Min ADC count	Max ADC count	Residuals
12 bit ADC Gpa 14 SSH 50ns LSB 4.3 mV	509 at 3 p.e.	3873 at 50 p.e.	from 21 to 54 UADC

Table 3.19. Setting value for charge measurements and the main results; 12-bit ADC.

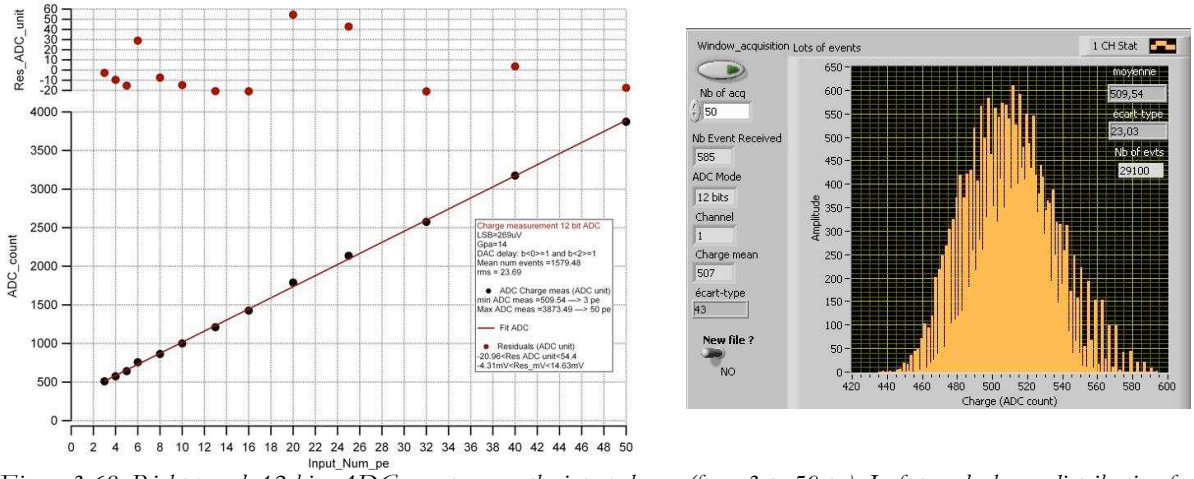

Figure 3.68. Right panel: 12-bit ADC count versus the input charge (from 3 to 50 pe). Left panel: charge distribution for channel one for 3p.e..

7.3. ADC measurements conclusions

The ADC test and the charge measurements showed nice results.
For the ADC performances:

- Good ADC uniformity among the channels with rms value from 0.5 to 1 UADC;
- A charge distribution for a single channel with spread of 5 UADC;
- An exact charge conversion measured with a DC level in the external ADC input;
- Good uniformity among channels;
- Good linearity (INL) with residuals better than 0.5% for the 8-bit ADC and 10 bit ADC and 1.5% for 12-bit ADC.

For the whole chain test:

- Linearity at 1.6% for the 8-bit ADC with noise of 1.53 UADC;
- Good linearity at 1.5% for the 10-bit ADC with noise of 6 UADC;
- Linearity at 1.6% for the 8-bit ADC with noise of 1.53 UADC;
- Linearity at 1.5% for the 12-bit ADC with noise of 23.69 UADC;
- Clock noise observed in channel charge distribution.

8. Time measurements

The chip time performances have been tested by IPNO team and are presented in this section.
A non linearity has been observed for the TDC ramp and this will be corrected in the second version of the chip explained in Chapter IV. Not considering this problem, each ramp has a time precision measurement less than 1ns. The fine and coarse time measurements will be explained in the next sub-section.

8.1. Fine time

The TDC has been reconstructed from the time values saved in the analog memory and converted by the ADC (10-bit).
A periodica pulse signal is injected into channel one; this signal has amplitude of 20 mV, rise time and fall time of 5 ns, and a period of 200 µs. The first signal is synchronized with the rising edge of the "start ramp" signal that allows the start of the TDC ramp, 10000 events are memorized. Then the signals are injected with a delay of 1 ns and synchronized.
The TDC ramp reconstructed is displayed in Figure 3.69. The blue curve is the TDC ramp stored on the first capacitance (C1) of the SCA cell and the red curve is the ramp stored on the second capacitance (C2).

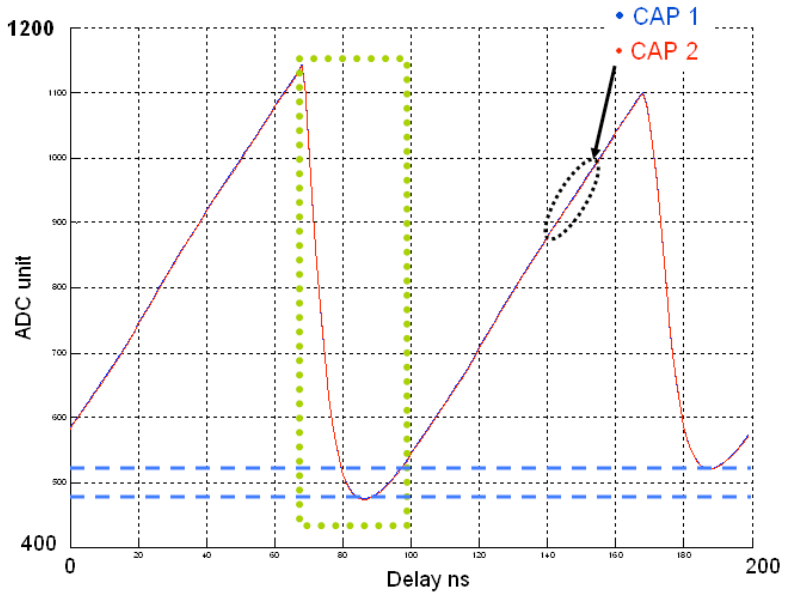

Figure 3.69. TDC ramp reconstruction by time values saved in the SCA of depth 2: capacitance C1 is the blue curve and and capacitance C2 the red curve.

The mean time dynamic range of the two ramps is about 622 UADC that correspond to 83 ns with a resolution of 133 ps. For an ADC of 10 bits the dynamic range is of 1023 bits thus only the 60% of the total conversion will be used with a worsening of the time precision.
The two ramps have an offset at the start and at the end of the ramps. This induces an error in the time measurement of 6 ns.
A "dead zone" exists between the two ramps of around 30 ns thus 30% of the overall ramp cannot be used to measure the time.
The linearity of the two ramps (the blue ramp and the red ramp in Figure 3.69) has been calculated considering the linear zone (between 95 ns and 165 ns) of 70 ns. Figure 3.70 illustrates the first ramp (Ramp1) linearity for the first capacitance (C1) and its residuals with values from -6 and 6.5 UADC then the time measurement error is of 918 ps.

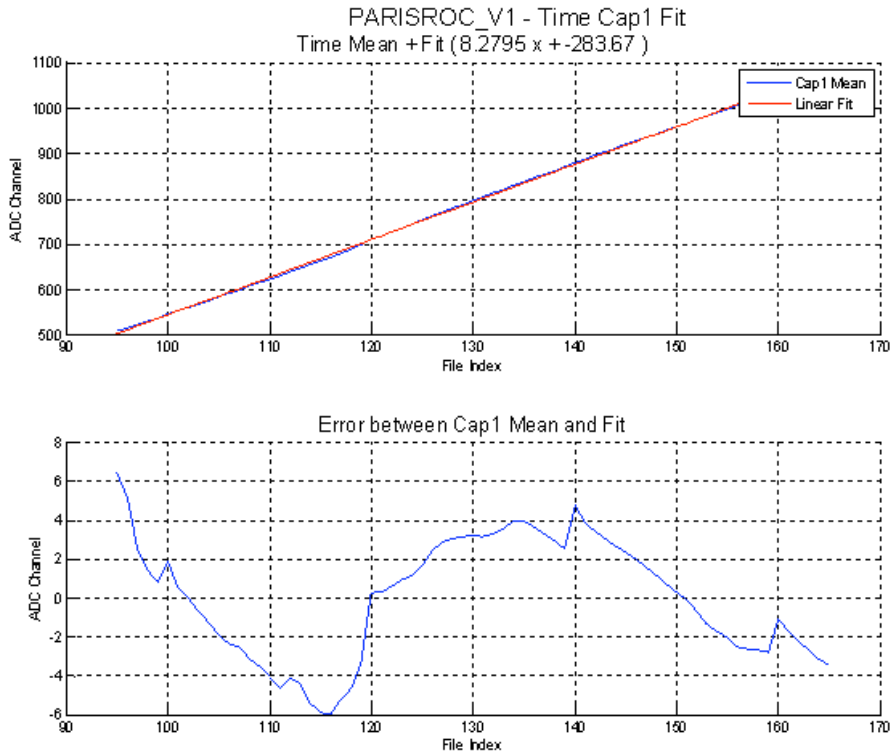

Figure 3.70. TDC ramp1 linearity C1 and residuals in UADC.

Table 3.20 lists the linearity results obtained for the two ramps and the two capacitances.

	Ramp 1		Ramp 2	
	C1	**C2**	**C1**	**C2**
Slope (ns)	8.3	8.3	8.3	8.3
Intercept (UADC)	- 284	- 285	- 1082	- 1083
Residuals (UADC)	- 6 to 6.5	- 6 to 7.5	- 6 to 8.3	- 6 to 9
Time error (ps)	785	918	1.1	1

Table 3.20. TDC Ramp linearity results.

The differences between the two ramps obtained with the values saved on C1 and C2 are plotted on the Figure 3.71. For Ramp 1 a mean difference of 1.88 UADC is obtained with a sigma of 0.5 UADC; for Ramp 2 the difference is 1.96 UADC with sigma of 0.45 UADC. This implies an error in time measurements with mean value of 2 UADC which corresponds to 242 ps.

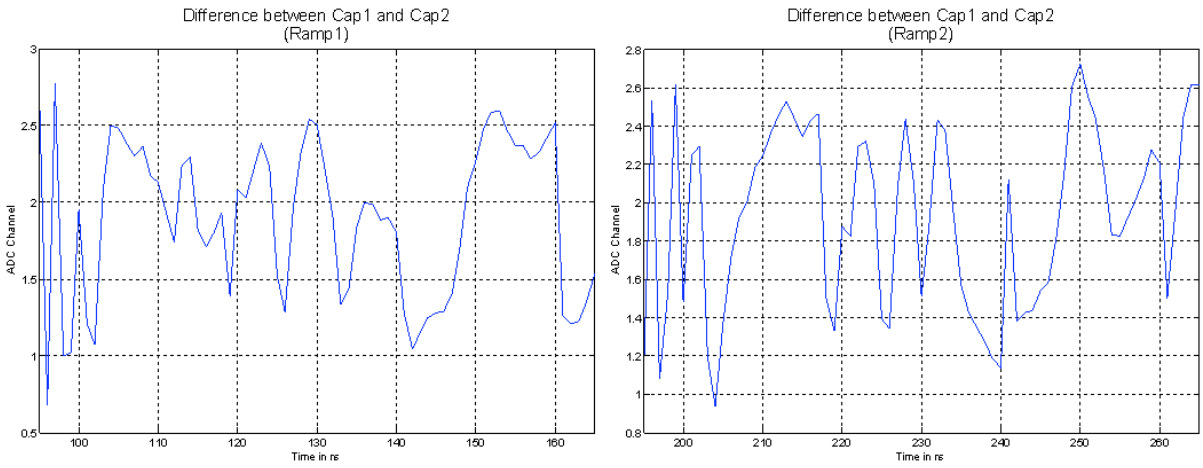

Figure 3.71. Difference between C1 and C2 of Ramp 1 (left plot) and of Ramp2 (right plot).

8.2. Coarse time

The coarse time obtained using the 24-bit counter has been tested. The same input signal of the previous section has been injected and the distribution of the time differences between the consecutive events has been plotted (Figure 3.72). As the input signal frequency is constant the difference between two events should be displayed in one ADC count. The spread on three ADC count indicates an error of ±1 LSB on the coarse time measurement. This error is due to the signal that arrives at the moment when the counter is changing its value. The probability of this situation is 0.4% on 1000000 events.

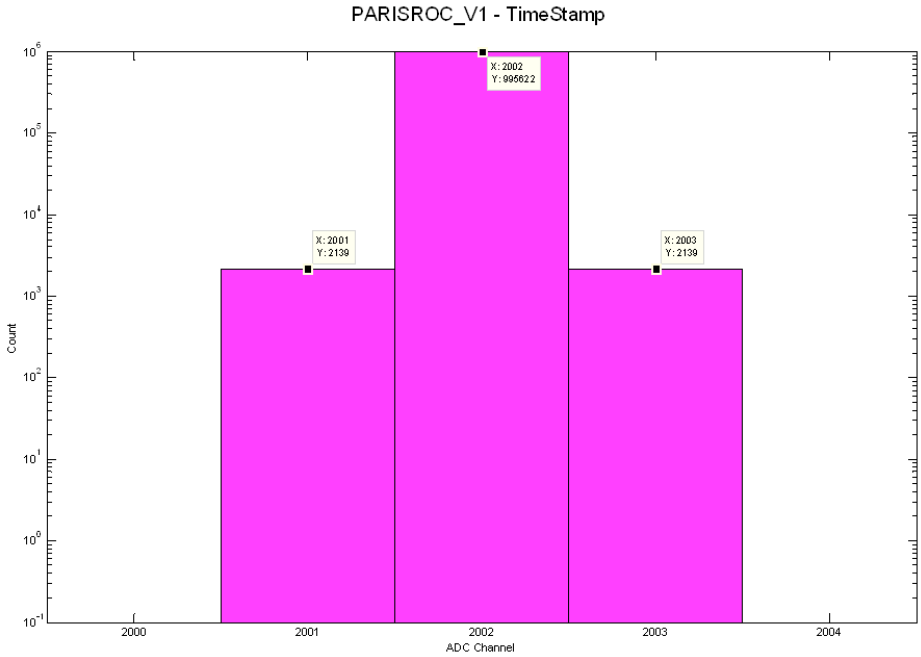

Figure 3.72. Distribution of the time differences between the consecutive events.

9. PMT measurements

The tests described until now on the PARISROC chip have been realized using a pulse generator input signal modeling the PMT signal at a gain of 10^6. The performance of the chip with a real PMT signal has been tested, since the single electron signal has a great dispersion in terms of charge and in shape. The chip has been tested in the Institute of Nuclear Physics laboratory (IPNO).
Using 10-inch (XP1804 Photonis) and 1-inch PMTs (XP3102 Photonis) the single photoelectron response has been reproduced with the internal ADC.
Some preliminary tests with the 10-inch and 1-inch PMTs confirm the presence of the noise observed in the chip tests described previously. The PMT measurements indicate that the chip can be used with a PMT gain of 10^7 to reach the chip requirements given by the project.

9.1. SET-UP measurements

Figure 3.73 represents the set-up diagram used in the measurements; the PMT is connected to the oscilloscope, to control the signal and to the chip input to process the signal. The chip output probe and discriminator output (trigger) are connected to the oscilloscope. The PMT signal is measured on a high impedance input of the oscilloscope to branch the same signal to the chip.

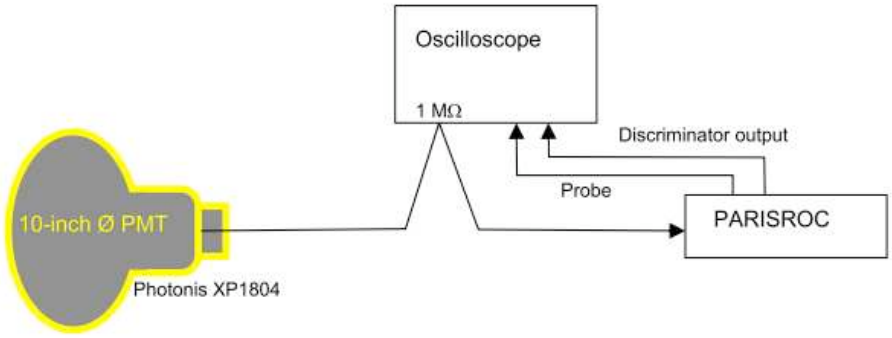

Figure 3.73. The set-up diagram: the PMT is connects to the oscilloscope, to control the signal and to the chip input to process the signal. The chip output probe and discriminator output (trigger) are connected to the oscilloscope.

The 10-inch PMT chosen for measurements has a dark noise of 1 kHz at room temperature with a dead time of 30 μs. The PMT, with a gain of 2.4 10^7 at a bias voltage of 1840 V, is placed in a dark box and the single p.e. signal from the noise is measured with the oscilloscope and is shown on Figure 3.74.

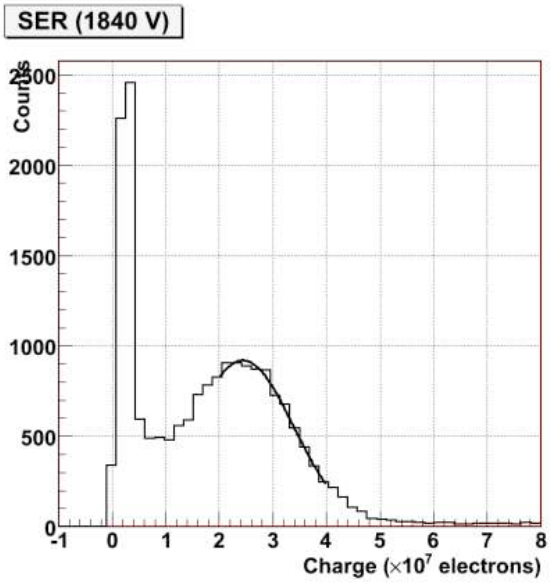

Figure 3.74. 10- Inch single electron response obtained from the noise (with a threshold set to 250 DAC channels) at a bias voltage of 1840 V measured with the oscilloscope. The relative RMS calculated from the gaussian fit (thick line on the histogram) is 0.38.

A good peak-to-valley ratio (P/V) has been obtained close to 2 and the rms calculated from the Gaussian fit (thick line on the histogram) is 0.38. Figure 3.75 shows on the top the 10-inch PMT signal acquired on the oscilloscope and at the bottom the trigger signal obtained with the chip.

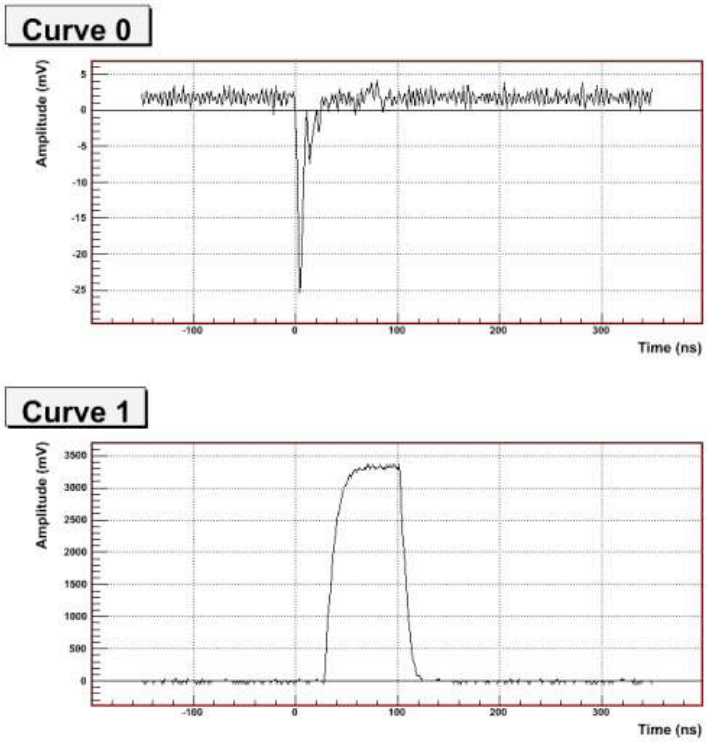

Figure 3.75. Top: the 10-inch PMT input signal on the oscilloscope; Bottom the trigger signal obtained with the chip.

The 1-inch PMT, used at a gain of 2.4 10^7 with a bias voltage of 1200V, has been tested and showed good performance in gain and time resolution. It is faster than the 10-inch PMT and has lower noise. The Figure 3.76 displays the single photoelectron signal obtained from the noise. The P/V has a value close to 2 with a resolution of 0.32.

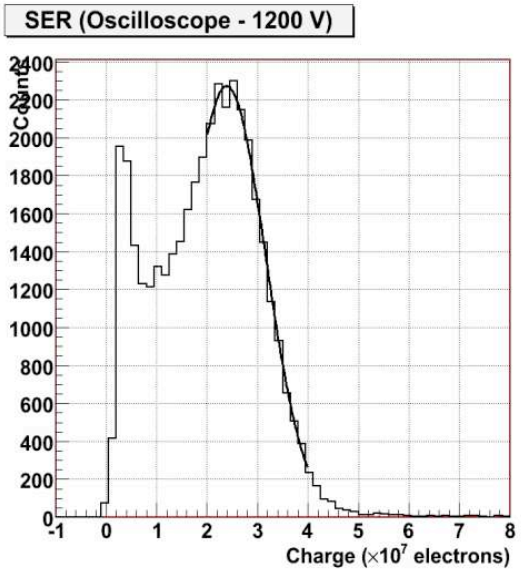

Figure 3.76. Single electron response of the 1-inch obtained from the noise (with a low discriminator threshold) at a bias voltage of 1200 V measured with the oscilloscope. The relative RMS is 0.32.

9.2. Slow Shaper performance

The chip performance has been studied comparing the single p.e. response obtained by the peak amplitude of the slow shaper signal and the same response obtained with the oscilloscope directly with the integral of the 10-inch PMT output. The Figure 3.77 shows the slow shaper output waveform for a 1 p.e. input signal after pedestal subtraction. The maximum value is measured fitting the signal around the peak with a parabola.

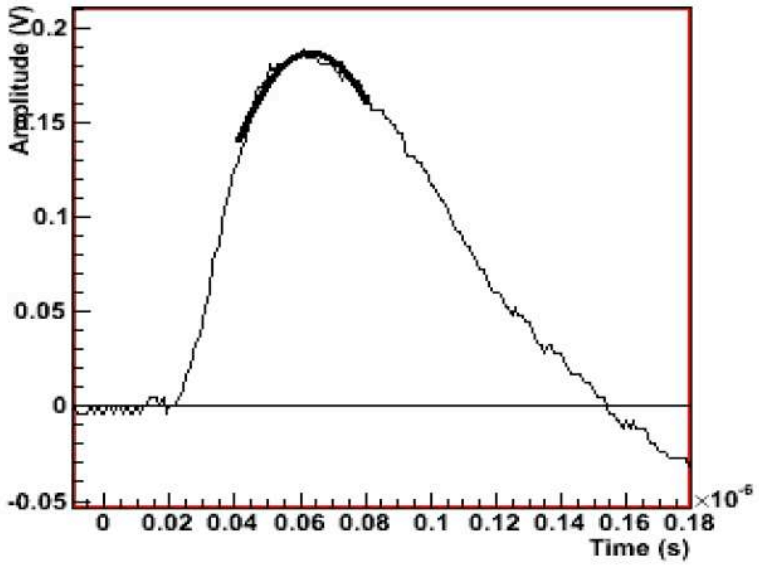

Figure 3.77. Typical shape of slow shaper signals with the fit (thick line) used to measure the amplitude and the eak position.

A good agreement is reached with the two methods. Figure 3.78 displays the two measurements: the red curve represents the measurements obtained on the oscilloscope with the PMT input signal and the black curve is obtained from the slow shaper amplitude.

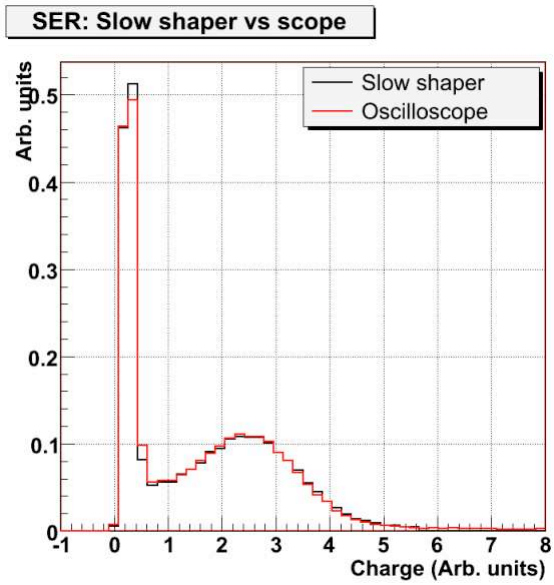

Figure 3.78. Comparison of the single p.e. responses of the 10-inch PMT obtained from the noise, with a threshold set to 250 DAC channels. Red line: signal integral (named "oscilloscope"in the legend). Black line: slow shaper amplitude rescaled from the Gaussian fit data (Figure 3.77). The relative RMS of the peak obtained with the slow shaper is 0.41.

9.3. ADC performance

Figure 3.79 shows the spectrum for a 10-inch PMT obtained with the 8-bit ADC and preamplifier input capacitor value of 4pF (Cin). The measurements with the PMT confirm the results obtained in the chip tests on the clock noise. However, since the pattern is periodical, 4 bin pattern (zoom on Figure 3.79), this can be corrected after measurements to hide this phenomena.

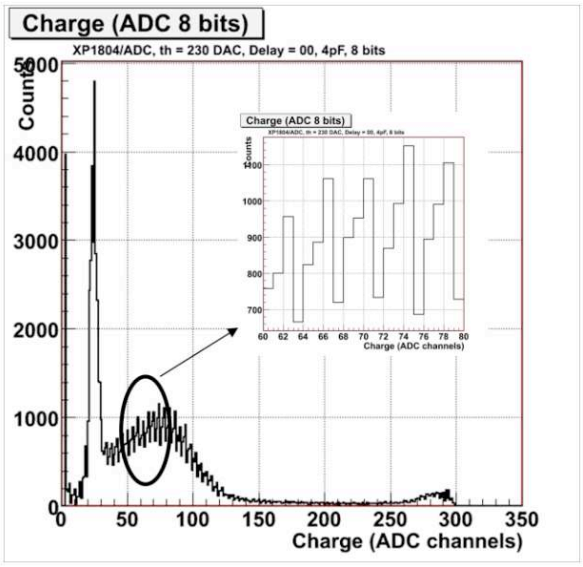

Figure 3.79. 10-inch PMT (PMT gain 2.4 10⁷): spectrum obtained with the 8-bit ADC and an input capacitance of 4 pF.

Good agreement in charge measurements has been obtained comparing the single p.e. response measured with the oscilloscope and with the ADC. Figure 3.80 shows in black the ADC measurements (the signal is auto-triggered and converted in digital data); in red the oscilloscope measurements and in blue the slow shaper ones. The single p.e. response from ADC conversion shows the sub-threshold events that could be due to events too close from one another: this phenomenon seems to appear when the instantaneous counting rate is too high.

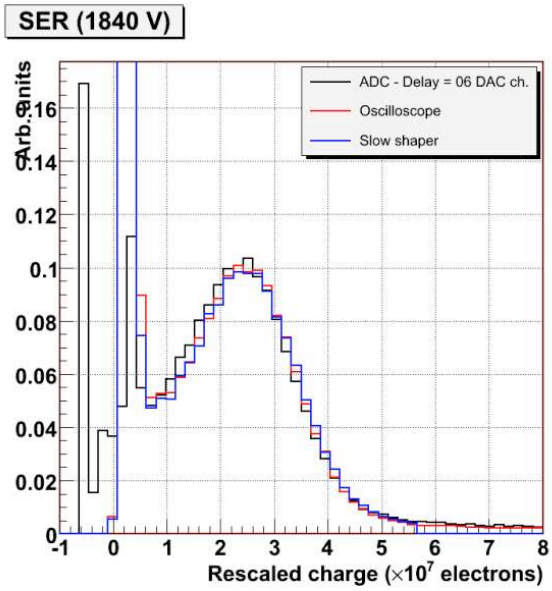

Figure 3.80. Comparison of the 10-inch PMT single electron responses measured with the ADC (Pedestal subtraction) and with the oscilloscope. PMT gain 2.4 10⁷

9.4. Time resolution

The time resolution is calculated measuring the difference between the trigger signal and the PMT signal (the arrival time).
With a 1-inch PMT, at a gain of 2.4 10^7, a time resolution of 600 ps RMS is obtained at a low threshold corresponding to 0.1 p.e. With a threshold of 0.3 p.e. the resolution shifts to 650 ps RMS.
Plotting the trigger arrival time versus the injected charge (Figure 3.81) a linear dependence of the arrival time with the charge is observed, except in the threshold region (< 0.3 p.e.) where there is an dramatic increase of the arrival time and of the dispersion.

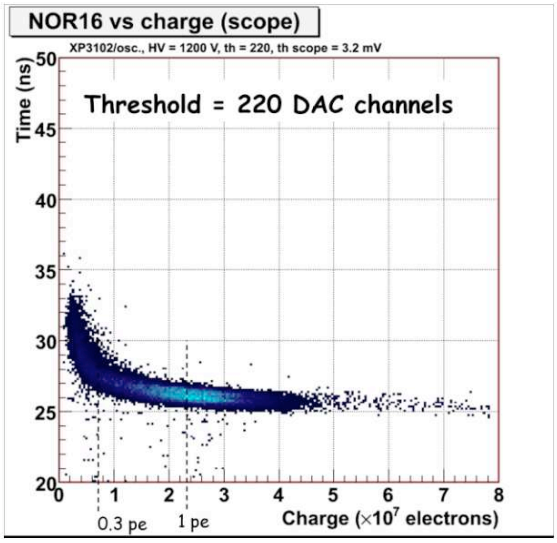

Figure 3.81. Time resolution measured with the 1-inch at a gain of 2.4×10⁷. The threshold is set to 220 DAC channels.

The 10-inch PMT has a degraded resolution: a RMS of 1.5 ns with a threshold of 0.3 p.e. Time versus injected charge (Figure 3.82) has also a different shape which is wider and with a slightly greater time walk (45 ns instead of 30 ns).

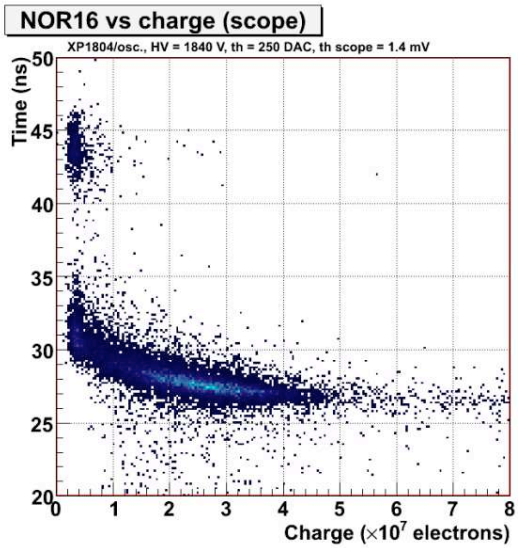

Figure 3.82. Time resolution measured with the 10-inchPMT at a gain of 2.4×10⁷at a threshold of 220 DAC channels.

9.5. 16 one-inch PMTs measurements

The preliminary tests of the ASIC and the DAQ were conducted with small PMTs: 16 1-inch PMTs (XP3102) have been tested with the PARISROC chip, the PMm² box (all in the pressure vessel) and the DAQ software. The 16 PMTs of 1-inch are placed in an array of 4*4 as shown on Figure 3.83 and all the PMTs have close gains except for the 13th channel. The gain is set at 2.4 *10⁷.

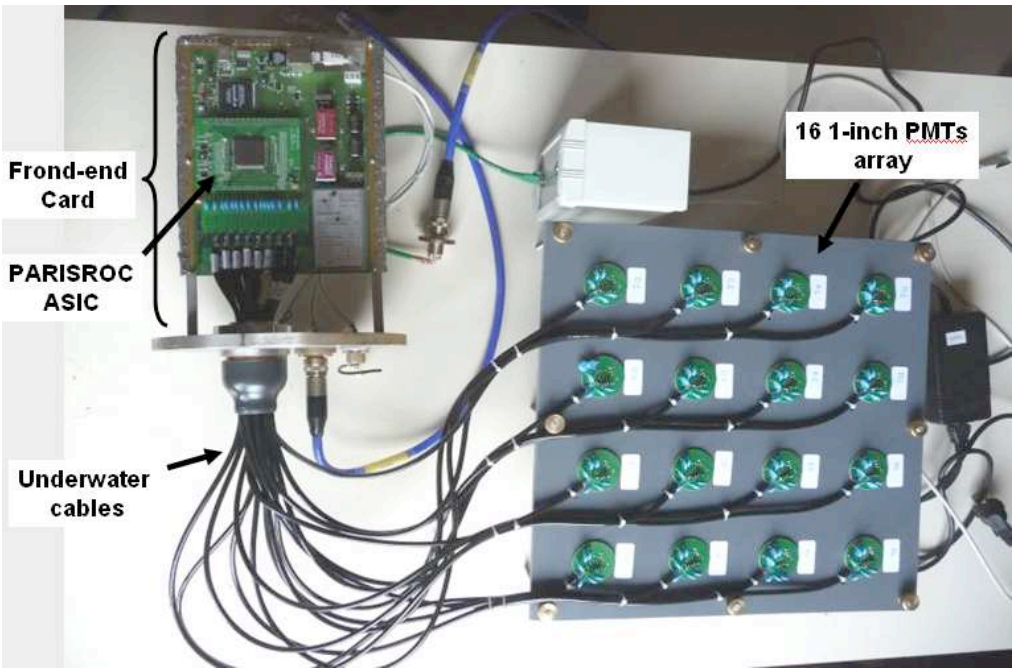

*Figure 3.83. The 16 PMTs of 1-inch are placed on an array of 4*4 and tested with the front-end realized at the IPNO, the PARISROC ASIC, the underwater cable and the DAQ.*

The DAQ software records the data before processing and analysis. The pedestal measurements and the single p.e. noise response are considered for the 16 channels test. The pedestal distribution is shown on Figure 3.84. It has a mean value of 240 ADC units (12 bit ADC) and a RMS value of 6.3 ADC units. The noise results in an important value: average of 16 ADC units with a RMS value of 4.5 ADC units.

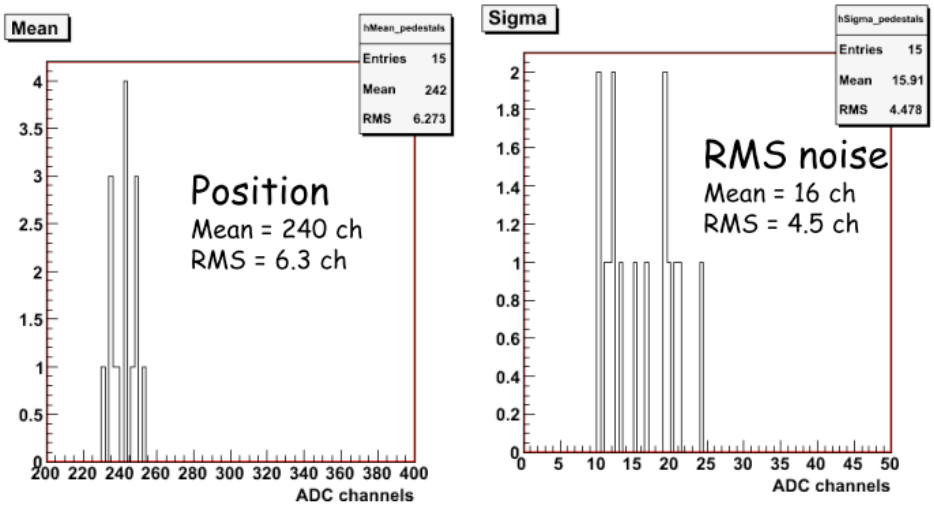

Figure 3.84. Pedestal distribution. Left: mean values (calculated by fit). Right: distribution of the RMS of the peaks (calculated by the fit).

Working at high PMT gains to find easily the single p.e. response (SER) peak, the ASIC gains were adjusted roughly.
Figure 3.85 shows the single p.e. response for each 16 channels after pedestal subtraction and gain matching. The threshold is placed at 0.2 p.e. and some events are observed under threshold. These events confirm the coupling signal observed in measurements.

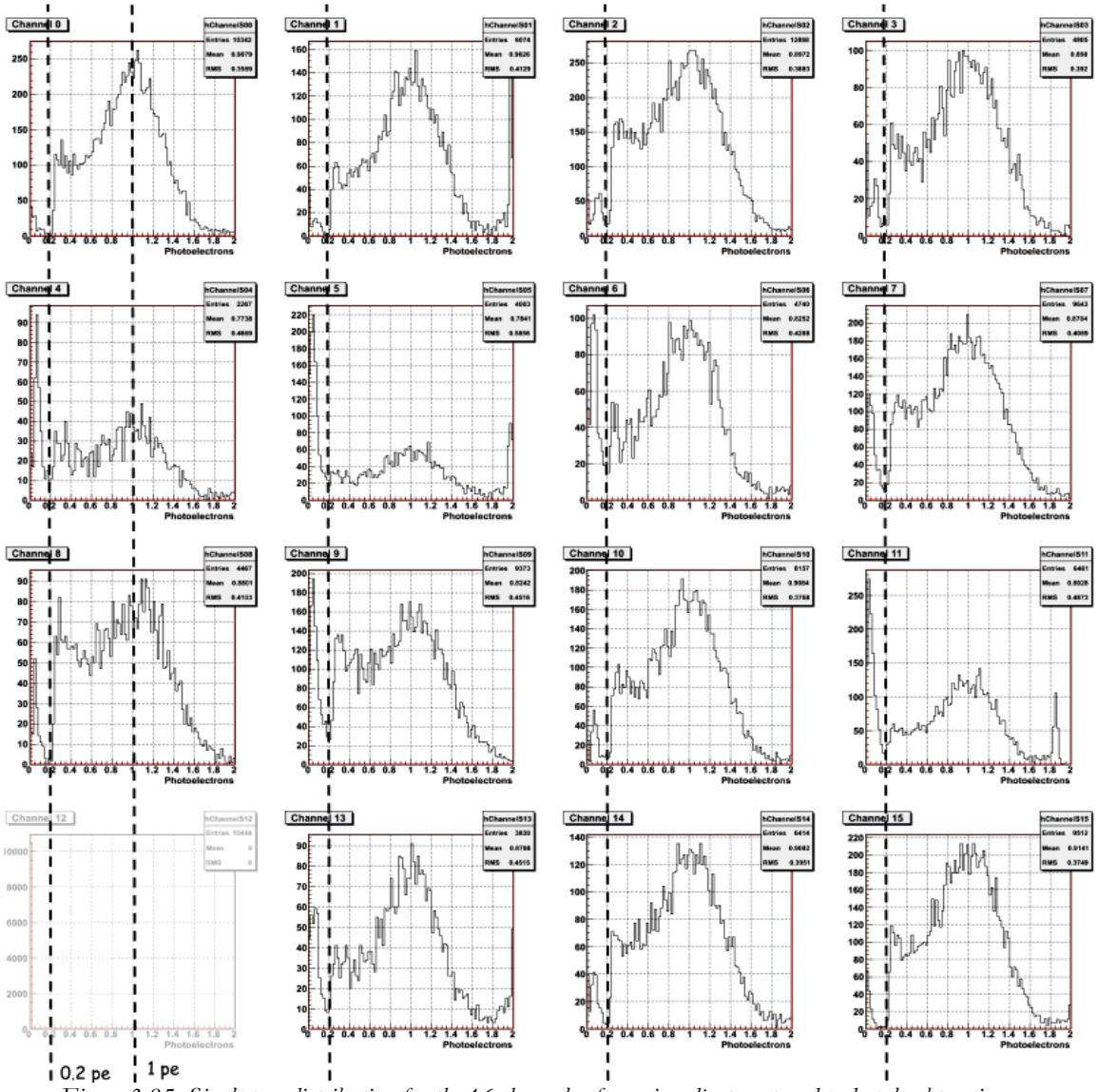

Figure 3.85. Single p.e. distribution for the 16 channels after gain adjustment and pedestal subtraction.

The gain alignment is calculated according to a given target for the mean single electron peak positions on Figure 3.85. Good performance of gain matching has been obtained has show on Figure 3.86. For all the 16 channels the charge values of 1 p.e. signal have been plotted, a good distribution with a RMS value of 38 ADC unit is obtained. The histogram is plotted after pedestal subtraction. The threshold is estimated in photoelectrons: it is about 0.2 photoelectrons.

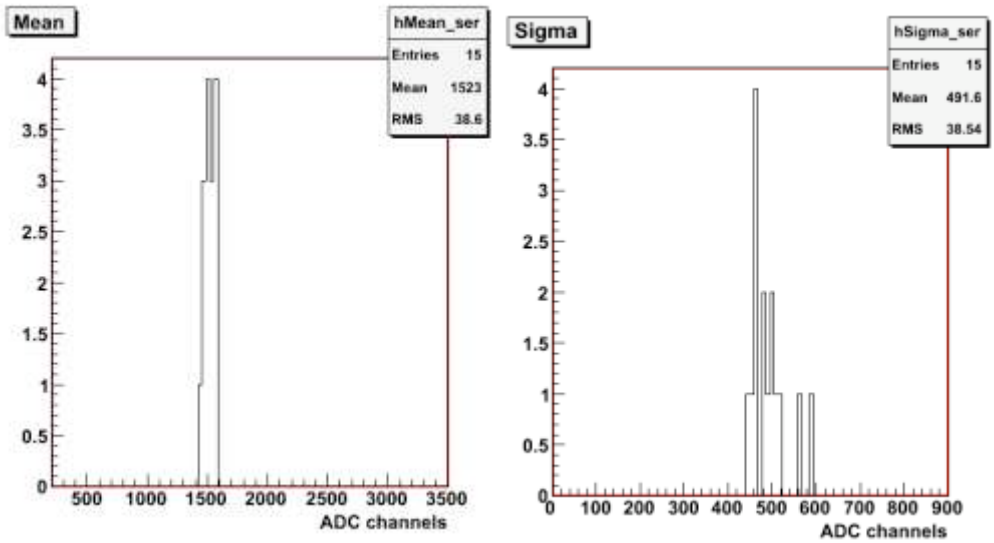

Figure 3.86. Statistics after gain matching. Left: 1 p.e. charge distribution; Right: RMS distribution of the charge.

10. Conclusions

The ASIC complexity has generated a significant number of tests that have brought to many important conclusions.
The ASIC has been conceived to operate as a self-triggered device, meaning that the chip can be autonomous and decide when to convert charge and time. The tests described in § 7.2 Chapter III, have shown that this functionality works: the input signal has given charge and time digitalized values.
The chip tests have shown:

- A clock coupling noise;
- An extra source of noise;
- A discriminator coupling signal that limits the minimum threshold at10 σ noise;

A second version of the ASIC has been conceived to solve the first version bugs.

Chapter IV

PARISROC 2

1. Introduction

A new version of the PARISROC ASIC has been designed to correct the bugs observed during the phase of measurements, to improve some analog blocks and enhance some chip performances.
Additionally, some important simulations [26], performed on the first version, have led to an understanding that the ASIC performance doesn't keep up with the rate of the PMT dark signal. These simulations, which explain the need for a new ASIC, will be described in the following section. The ASIC modifications and the improved measurements will be presented in this chapter.

2. Motivation for a new version

As demonstrated in the chapter III, an improvement of the ASIC was necessary in terms of noise performance and of threshold setting, whereas the measurements made with a PMT connected in the input indicate that the ASIC works[54] performing charge and time measurements as explained in § 9 Chapter III
Another problem has been noticed in a specific simulation [24] performed to investigate the loss of physics events attended using the ASIC.
The physics events in a Cerenkov detector have a rare occurrence (§ 6 Chapter I) therefore only some p.e. per MeV can be detected by one PMT, then, its signals are dominated by the noise. The main sources of PMT noise are the thermo-emission from the photocathode and dynodes and the external or internal radioactivity that create extra low signals in the PMT output. These signals cannot be distinguished from real events.
The dark noise rate estimated for the PMT used in the PMm² program is about 5 kHz (up to 10 kHz) thus the ASIC will have continuous input signals with this rate in all its 16 channels.

From § 4.4 Chapter II, it is known that the ASIC has an analog memory with depth of two; two capacitances allow store the measurements of charge and time that are treated in ping–pong mode. When the signals are injected into the 16 channels, they are saved first in the depth one of the analog memory. These signals are treated in parallel by the digital part and the total time of conversion is given by:
$T_{cycle} = T_{wait} + T_{conv} + T_{RO}$
Where

- T_{wait} is a fixed time of 200 ns imposed by the digital part before starting the conversion;

[54] The measurements work with high PMT gains (10^7).

- T_{conv} is the time of conversion given by: $T_{conv} = \frac{2^n}{F_{conv}}$ that depends on:
  - The number of ADC bits (n);
  - The conversion frequency (F_{conv}) (nominal value 40 MHz).

  Considering that the maximum number of the ADC bits for the PARISROC ASIC (version one) is 12, the maximum time of conversion will be of order 102 μs.
- T_{RO} is the time of readout given by $T_{RO} = T_{RO,over} + n_{hits} \times T_{RO,hitsf}$ where:
  - $T_{RO,over}$ (overhead) is the minimum time of readout that can be calculated by $T_{RO,over} = 16 \times 10 \times \frac{1}{F_{RO}}$ that depends on:
    - The readout Frequency (F_{RO});
    - The two constants 16 and 10 that indicate respectively the number of chip channels and the number of clock ticks need to process each channel.

    For a readout frequency of 10 MHz $T_{RO,over}$ is equal to 16 μs.
  - $n_{hits} \times T_{RO,hitsf}$ depends on:
    - n_{hits} (the number of channel hits),
    - The number of output data bits and the readout frequency: $T_{RO,hitsf} = \frac{N_{bitsData}}{F_{RO}}$ (5.2 μs for 52 bits of data).

During this T_{cycle} the other signals injected into the 16 channels can be saved in the second capacitor of the analog memory.
For different values attributed to these parameters and to various PMT noise, the simulation gives the results listed in Table 4.1. The one evidenced in blue and in pink correspond to the state of the PARISROC ASIC respectively in the first and in the second version. The first version has a loss of events that depends from the ADC bits and is around the 16 % for a 12-bit ADC and 6 % for a 10-bit ADC.
The improvements can be obtained principally:

- Decreasing the PMT noise rate that depends on the PMT qualities;
- Modifying the conversion which means decreasing the ADC bits or increasing the readout frequency;
- Changing the analog memory by increasing its depth.

Among these various hypotheses, the modification of the ADC bits and the readout frequency were chosen to design the second version of the ASIC. These lead to a loss rate of 0.3 % as indicates on Table 4.1. The increase of the SCA depth has been excluded because it leads to increase the die area and the complexity of the digital part.

Noise rate	Number of SCA capacitances	ADC bits	readout frequency	Lost events (%)
5 kHz	2	12	10 MHz	16 ± 12
0.1 kHz	2	12	10 MHz	0.008 ± 0.6
5 kHz	2	10	10 MHz	6 ± 10
5 kHz	4	12	10 MHz	3 ± 6
5 kHz	4	12	20 MHz	1 ± 4
5 kHz	4	12	40 MHz	0.3 ± 2.0
5 kHz	4	10	10 MHz	0.3 ± 2.2
5 kHz	4	10	40 MHz	0.007 ± 0.5
5 kHz	2	8	40 MHz	0.24 ± 3.1
5 kHz	4	9	40 MHz	0.007 ± 0.7

Table 4.1. Estimation of lost events. In the 1st column the noise rate, in the 2nd the number of capacitances included in the analog memory, in the 3rd the number of ADC bits, in the 4th the readout frequency and on the 5th the estimation in % of the lost events.

3. ASIC modifications

Numerous modifications have been done in the design of the second version of the PARISROC ASIC (named PARISROC 2):

1. The simulations described previously (§ 2 Chapter IV) have demonstrated that to reduce the events loss, a reduction of the ADC bits and an increase of the readout frequency at 40 MHz are required. This generates a modification of the digital part;
2. The ADC bits reduction results in degradation of the charge measurement precision. A modification of the input stage has been realized to preserve it. Two preamplifiers with different gains have been designed in each channel to split the input dynamic range in two parts; the small and the large signals are amplified respectively by a preamplifier with a high and low gain;
3. To solve some noise problem the input variable capacitor has been replaced by a capacitor with a fixed value;
4. Some improvements have been studied to improve the slow shaper noise performance;
5. The implementation of the two preamplifiers has induced a consequent modification of the charge analog memory;
6. The TDC ramp measurements, illustrated in § 8.1 Chapter III, indicate a poor linearity and an excessive dead zone. The TDC ramp has been improved and this has implied some modifications on the time analog memory.

The main conception of an auto-trigger ASIC with 16 channels that work independently and are managed by a common digital part has been preserved.
The global schematic is displayed in Figure 4.1 where are illustrated the general schematic of the analog channel, the common blocks to the 16 channels and the digital part.
The major modifications will be explained in this section with some primary simulations such as:

- The verification of the output waveforms;
- The rms noise performances;
- The linearity.

All the simulations described have been performed with the same input signal used with the PARISROC 1 ASIC (§ 3.1 Chapter II).

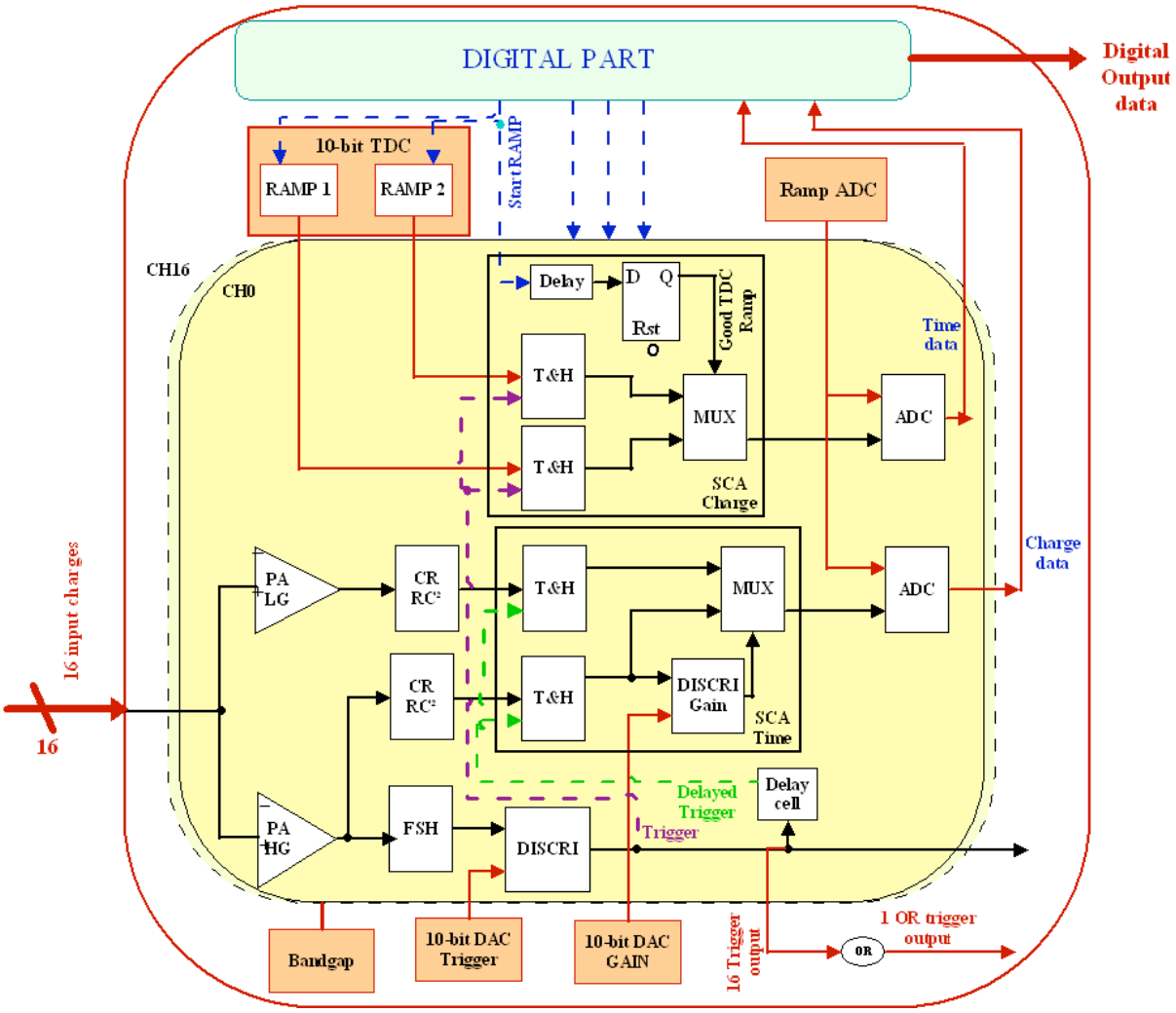

Figure 4.1. PARISROC 2 general schematic. Green block: the digital part; yellow block: analog part; orange blocks: 16 channels common blocks.

3.1. Digital part

The main modification in the second version of the PARISROC ASIC has been realized on the digital part and its main goal is the speed increased, by a factor of 4, of the trigger's treatment as listed on Table 4.2.

As conversion and readout take about 99% of the total cycle length, it has been decided to improve these two processes.

First, for the conversion, it has been demonstrated that the fine time resolution (less than 1 ns) can be achieved with a 10-bit ADC. But, for the charge, 2 gains have been added in the analog part to fulfill the precision on the entire dynamic range (0-300 pe) with this reduced number of bits. So, the ADC is now counting 10 bits: this allows dividing by 4 the time for the analog to digital conversion compared to PARISROC 1.

Secondly, the readout frequency has been increased to 40 MHz (multiplied by 4) and the number of bits in the readout frame has been slightly decreased thanks to a lower number of bits in the conversion. The readout frame, given below (Table 4.3), is composed of 51 bits for each channel.

All these timing improvements are shown in Table 4.2. They are compared to the first version of the ASIC in the worst case. We can expect a gain of a factor 4 on the total cycle length and we will be able to manage a 20 kHz hit rate on each channel with these new improvements.

	PARIROC version 1	PARIROC version 2
Time of conversion	103 us	26 us
Time of readout	101 us	25 us
Total cycle duration	204 us	51 us

Table 4.2. Worst case timing analysis

The worst conversion time is given by the overflows of the 10-bit ADC counter at a frequency of 40 MHz. The maximum readout time appears when all channels are triggered and with a readout frequency of 40 MHz.

Moreover, for this new release, it has been also integrated a completely new timing module which includes a new fine and coarse time measurement. This will allow tagging events with an increased accuracy and to remove the blind zones seen on the measurements of PARISROC 1 (§ 8 Chapter III).
First, for the fine time, we have chosen to have 2 independent ramps with an overlap between them. These 2 ramps will be sampled at the same time and an internal module will tag the valid one. Finally, the digital part will convert and readout the selected ramp. This is represented in Figure 4.2.

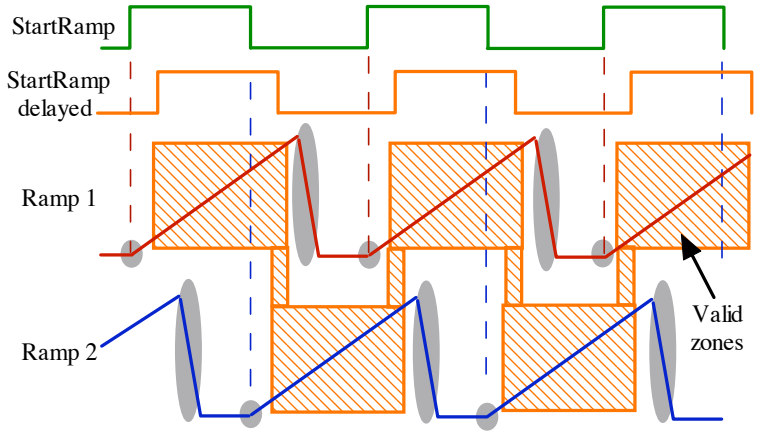

Figure 4.2. Overlap of TDC ramps.

The module that allows the validation of the good ramp is shown on Figure 4.3. A signal has also been added to enable the possibility to force the selected ramp.

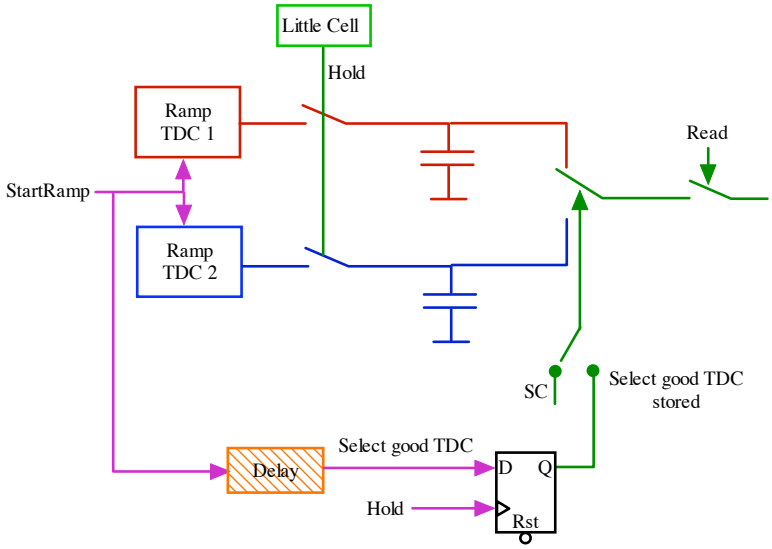

Figure 4.3. New fine time architecture with validation module.

In addition, the coarse time counter is now enhanced: it is able to detect triggers synchronous with the clock. This is done by using an extra 1-bit counter counting at the opposite edge of the clock. This counter is redundant with the least significant bit of the coarse counter and allows to correct it offline. Figure 4.4 illustrates the new coarse time architecture with the clock signal (green), the 24-bit and 1-bit counters (orange curves), the two TDC valid zones of time measurements (red and blue curves).

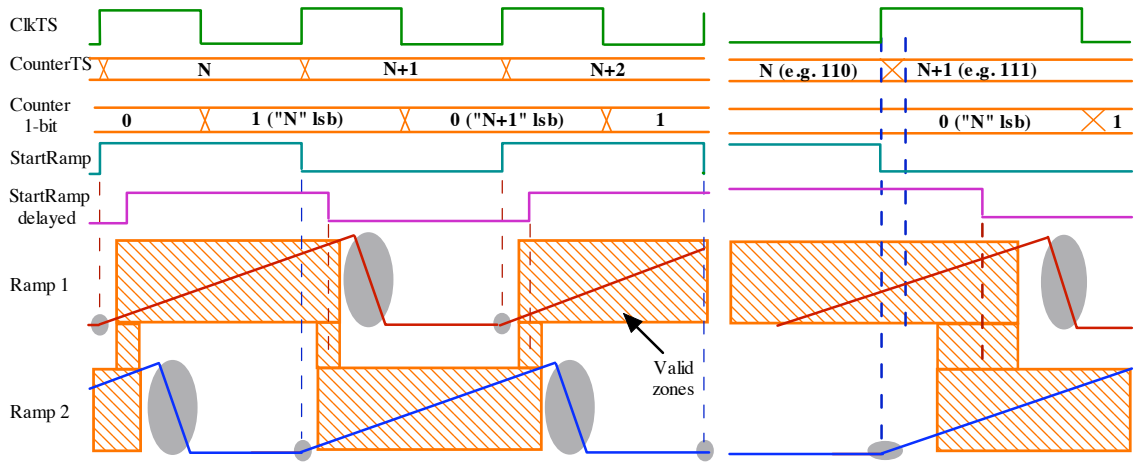

Figure 4.4. New coarse time architecture

The readout frame is given below in Table 4.3. It shows also the main difference between the 2 PARISROC releases. The main differences are due to the integration of the new time module (fine and coarse time) and the use of 2 gains in the analog part for charge measurement.

	PARIROC version 1	PARIROC version 2
Channel number	4	4
Coarse time counter	24	24
Extra Coarse time	NA	1
Gain used	NA	1
Charge converted	12	10
Fine time (TDC) used	NA	1
Fine time (TDC) converted	12	10
Total	52 bits	51 bits

Table 4.3. Number of bits in the readout frame.

3.2. Preamplifier

Two preamplifiers with different gains have been designed in each channel to split the input dynamic range in two parts. The utility of this separation comes from the requirement, as explained in the introduction, to have a reduction of the ADC bits and the necessity to preserve a good precision.
The preamplifier schematic has not been modified (§ 3.2.1 Chapter II) except for the input capacitance; the significant quantity of measurements made and explained in Chapter III have demonstrated that extra noise was injected by the power supply connected to the Cin switches therefore the variable capacitor Cin has been replaced by a single capacitance without a switch.
Figure 4.5 shows the general schematic of the two preamplifiers. The low and high gain preamplifiers have an input capacitance with fixed value respectively of 5 pF and 0.5 pF. Moreover, they have a variable feedback capacitance (on 8 bits) with default value of 0.25 pF. Therefore the two preamplifiers have a gain ratio of 10. The voltage references of the preamplifier and the OTA (named Vref_pa and Vref_OTA) are provided by a common bandgap like in the first version.

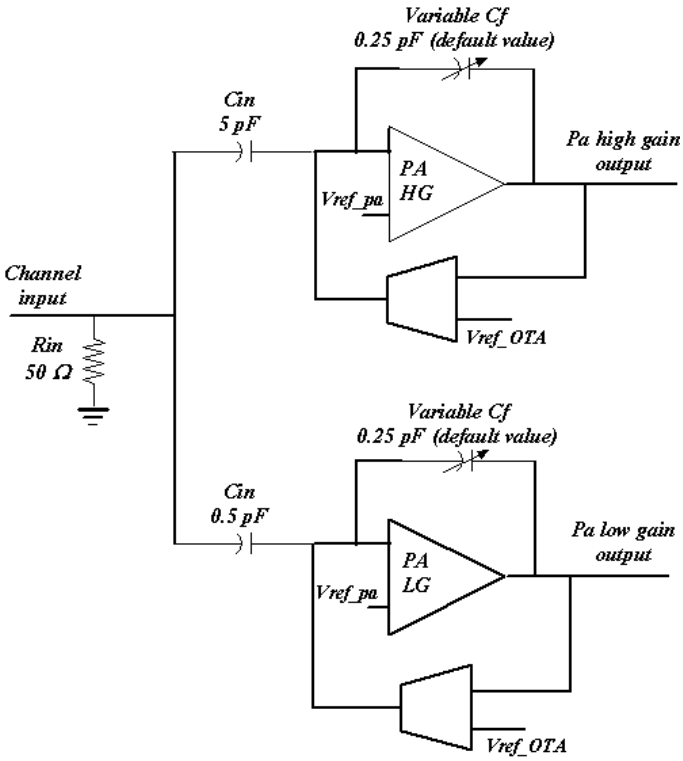

Figure 4.5. One channel preamplifier general schematic. HG and LG stand respectively for High and Low Gain.

The output waveforms for each preamplifier have been simulated with 1 p.e input signal; these signals are shown in Figure 4.6 and Figure 4.7 and indicate that for the low (2) and high (20) gain the preamplifier response is respectively 1.3 mV and 12 mV.

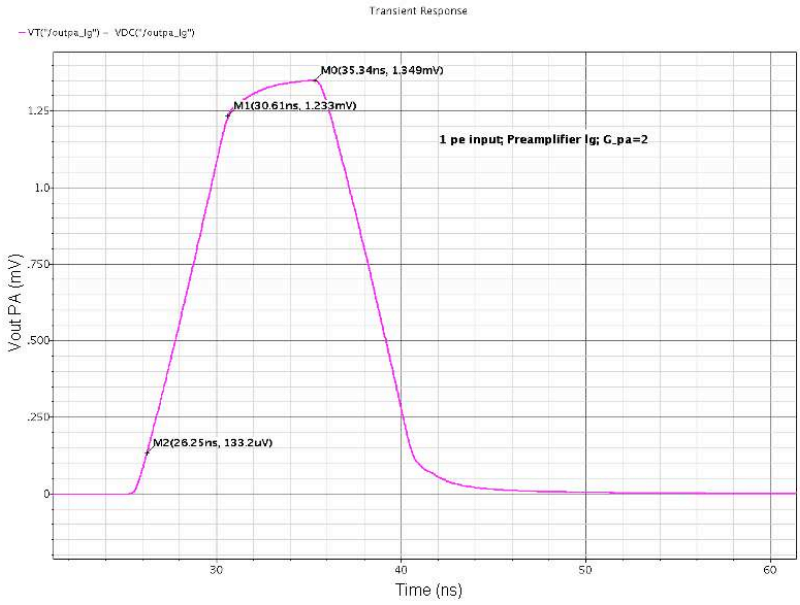

Figure 4.6. Simulated preamplifier low gain (2) output waveform for an injected charge of 1 p.e.

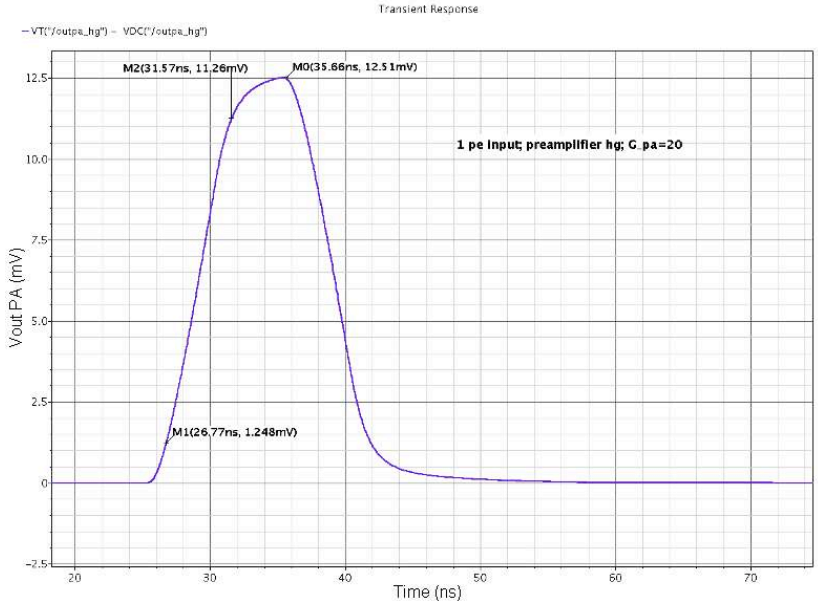

Figure 4.7. Simulated preamplifier high gain (20) output waveform for an injected charge of 1 p.e.

The noise performance has been simulated obtaining the equivalent preamplifier output noise curves illustrated in Figure 4.8 (low gain) and Figure 4.9 (high gain). The calculated rms noise values at 10 MHz give respectively 487 μV and 609 μV for low and high gain. These values are similar to the ones obtained in simulation in the first version (470 μV).

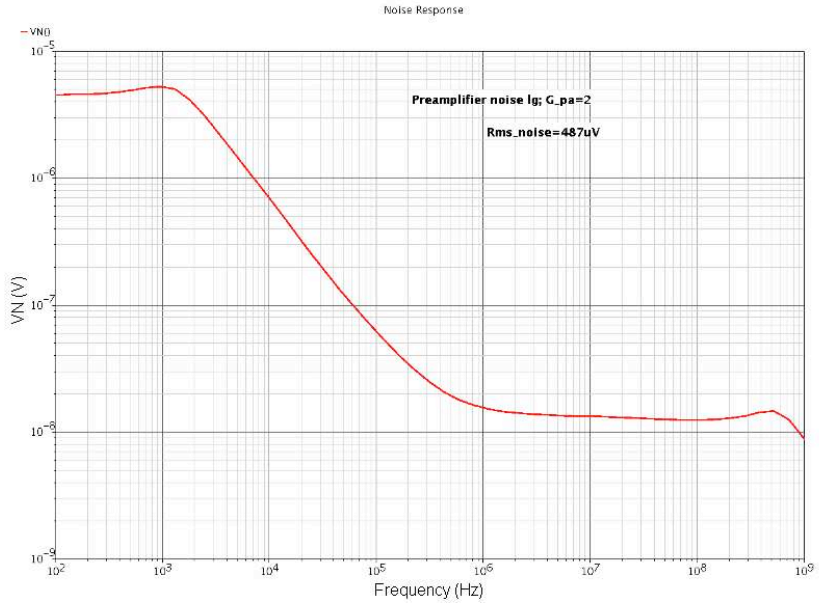

Figure 4.8. Simulated preamplifier low gain output noise. Rms noise at 10 MHz: 487 μV.

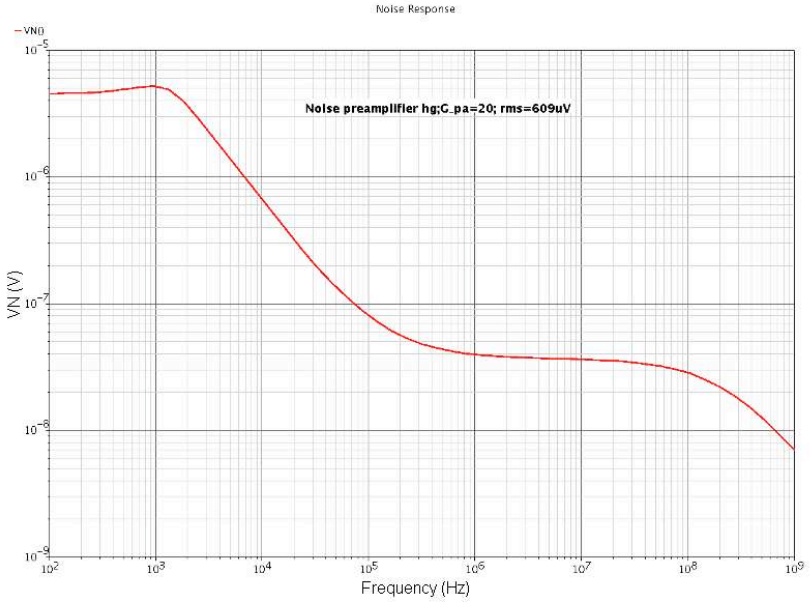

Figure 4.9. Simulated preamplifier high gain output noise. Rms noise at 10 MHz: 609 μV.

Finally the linearity has been investigated for the two gains injecting the dynamic range required by the physics events i.e. from 0 to 300 p.e. The plot in Figure 4.10 illustrates the linearity for the two preamplifiers; the red and blue curves correspond respectively to the high and low gain preamplifier.
From the figure can be deduced that the preamplifier high gain saturation is reached around 120 p.e. while no saturation is observed in low gain. The definition of the dynamic range for each preamplifier which can be extrapolated by the linearity is an important characteristic. Figure 4.11 illustrates the two linearities separately and the calculated corresponding residuals. The linearity simulations indicate that the preamplifier with high gain can work up to 90 p.e. with a good linearity better than 0.4 % and the preamplifier with low gain can cover the whole dynamic range with a linearity better than 0.6%.

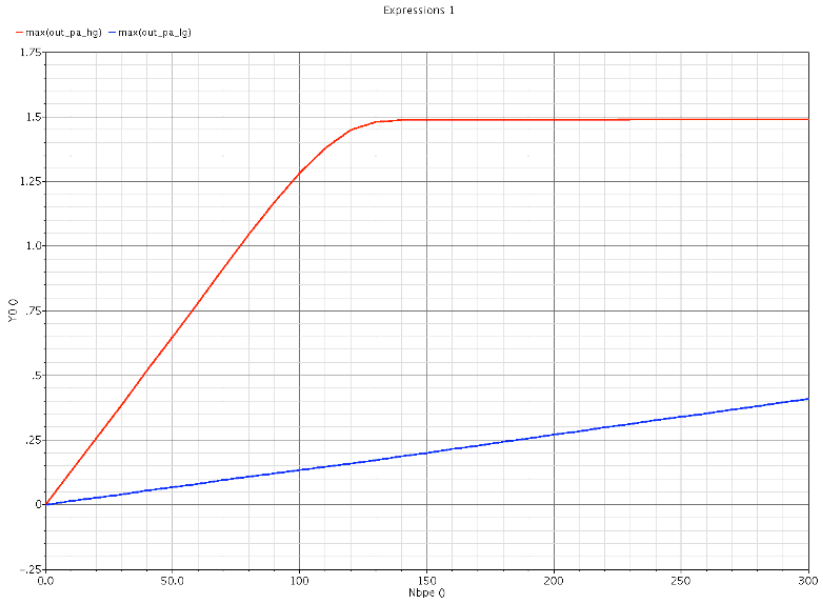

Figure 4.10. Simulated preamplifier linearity. The red and blue curves indicate the linearity respectively for high and low preamplifier gains.

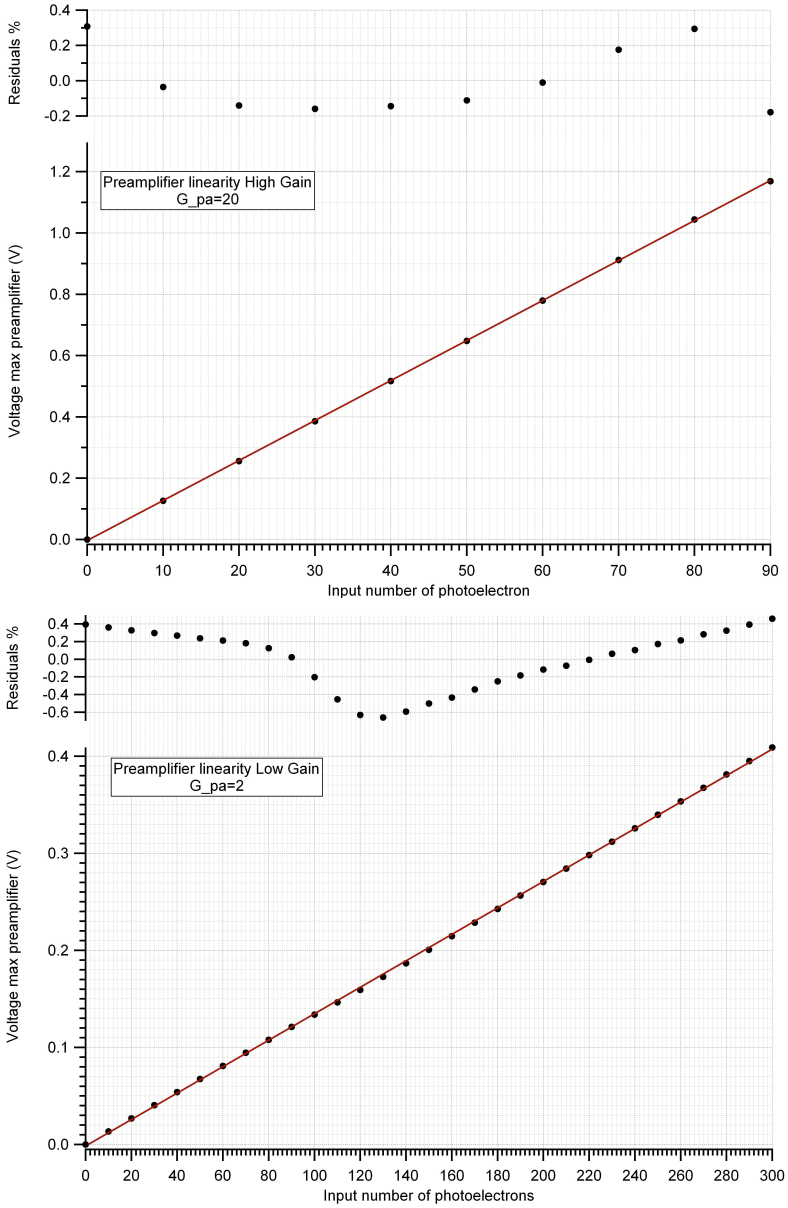

Figure 4.11. Simulated preamplifier linearity. The top and bottom plots represent respectively the low and high gain preamplifier linearity until 90 p.e. and for the whole dynamic range required.

3.3. Fast channel

The signals amplified by the two preamplifiers follow different channels:

- The high gain preamplifier output signal is sent in two channels in parallel the fast and slow ones;
- The low gain preamplifier output signal is sent only in a slow channel.

The fast shaper schematic is not changed and the main characteristics have been simulated. The fast shaper output signal is shown in Figure 4.12; an injected charge of 1 p.e. gives an output signal of 106 mV.

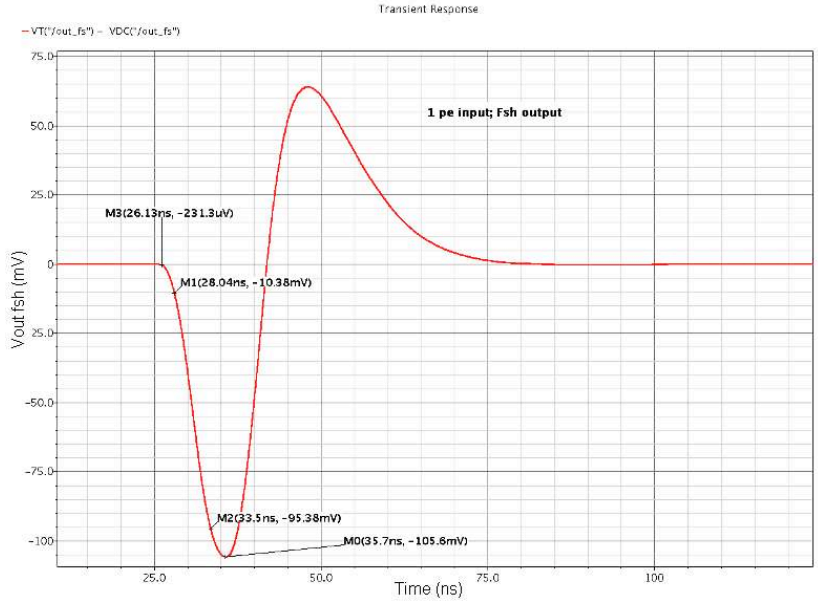

Figure 4.12. Simulated fast shaper output signal for an injected charge of 1p.e. and preamplifier gain of 20.

The fast shaper output equivalent noise is simulated and the curve obtained is displayed on Figure 4.13. The rms noise calculated at 10 MHz gives a value of 3.4 mV. Therefore with 106 mV of output signal for 1 p.e. the signal to noise ratio is 31 which is doubled with respect to the one of the first version.

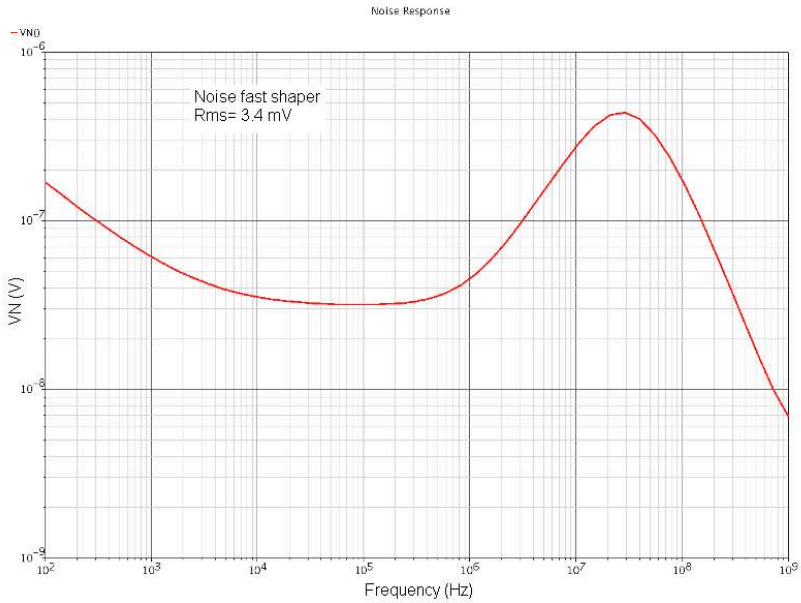

Figure 4.13. Simulated fast shaper equivalent output noise. Rms noise at 10 MHz: 3.4 mV.

The fast shaper signal is then sent to the discriminator (Figure 4.14) to create the trigger. Similarl to the first chip version, this signal is calibrated and produced with and without a delay respectively for the charge and the time measurement SCA channels.

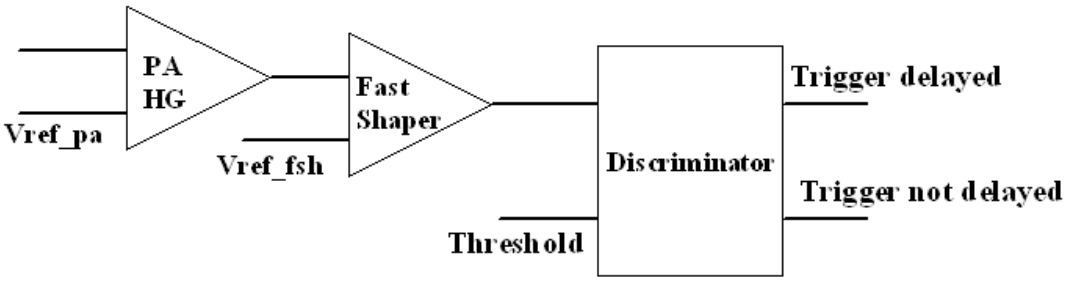

Figure 4.14. Fast channel general schematic.

3.4. Slow channel

The slow channel is made by two slow shapers dedicated to the high and low gain preamplifiers. The first chip measurements indicated high rms noise value for the slow shaper. Therefore the schematic of this block has been modified for the second version.
The new structure is illustrated in Figure 4.15; it is a typical CRRC² with variable peaking time that can vary from 25 ns to 100 ns. The main modification is that the gain can change by the feedback variable resistance Rf1. The slow shaper parameters are listed in Table 4.4.

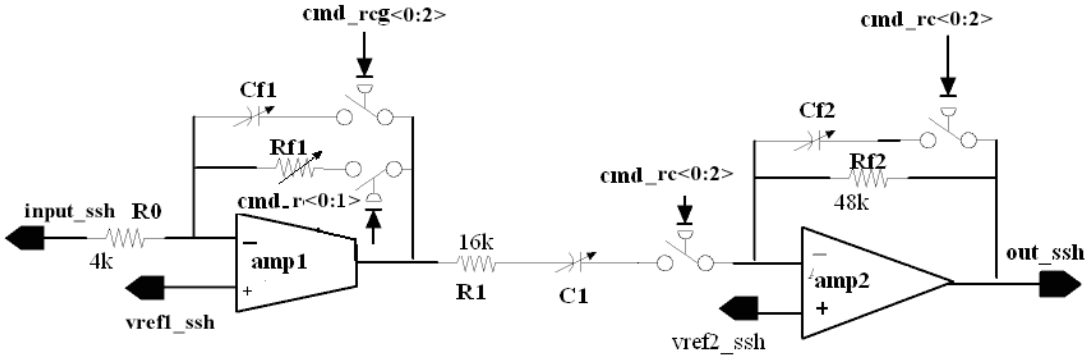

Figure 4.15. The slow shaper general structure.

Time constant (ns)	Rf1 (Ω), Cf1 (pF)	Vref1 (V)	Vref2 (V)	R1 (Ω), C1 (pF)	Rf2 (Ω), Cf2 (pF)	Gain of shaper
25	16K, 1.5625	1.21	1	16K, 1.5625	48K, 0.5208	0.9
50	16K, 3.125	1.21		16K, 3.125	48K, 1.0416	0.5
	32K, 1.5625	1.12				1
100	16K, 6.25	1.21		16K, 6.25	48K, 2.083	0.25
	64K, 1.5625	1.06				1

Table 4.4. Slow shaper parameters: shaping time, feedback resistors and capacitors values, voltage reference levels and shaper gains.

The 1 p.e. response and the rms noise (at 10 MHz) for the different parameter combinations have been simulated and are listed in Table 4.5. The rms noise ones, in all the cases, have values less than 1 mV indicating good performance with respect to the first slow shaper version which showed values higher than 1 mV (§ 4 Chapter III). Figure 4.16 displays an example of slow shaper output waveforms for an

injected charge of 1 p.e., a shaping time of 50 ns and gain 0.5. The pink and green curves correspond to the output signal of the high (20) and low (2) gain channels respectively.

Time constant (ns)	Gain of shaper	Rms Noise (μV) HG/LG	Peaking time (ns)	Maximum voltage at 1 p.e. (mV) HG/LG	SNR HG/LG
25	0.9	730 630	23.3	11 2	15 3
50	0.5	630 560	38.6	6 670 μ	10 1.2
	1	770 590	38.6	11 1	14 1.7
100	0.25	560 500	68.1	3.5 360 μ	6 0.7
	1	750 550	68.1	11 1	15 1.8

Table 4.5. Simulation results for the different parameters. The high gain and low gain correspond respectively to the preamplifier gain of 20 and 2.

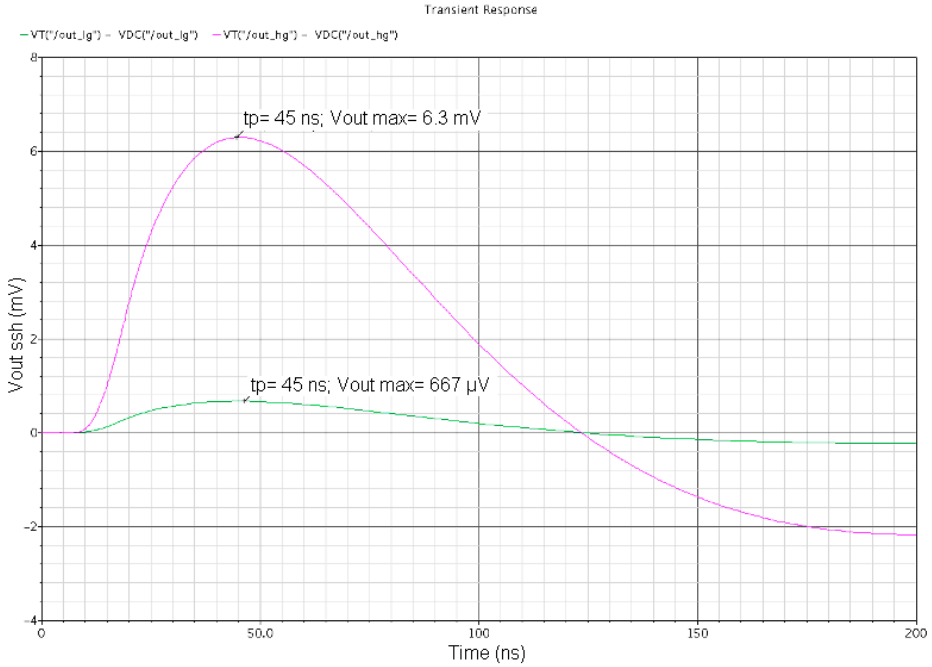

Figure 4.16. Simulated slow shaper output waveforms for shaping time of 50 ns and gain 0.5. Injected charge of 1p.e. Pink: high gain (20) slow shaper output; Green: low gain (2) slow shaper output.

The linearity has been investigated for the two slow channel gains for a shaping time of 50 ns and gain 0.5. The plot in Figure 4.17 displays the slow shaper linearity for the two channels; the red and blue curves represent the simulation respectively for high and low gain.

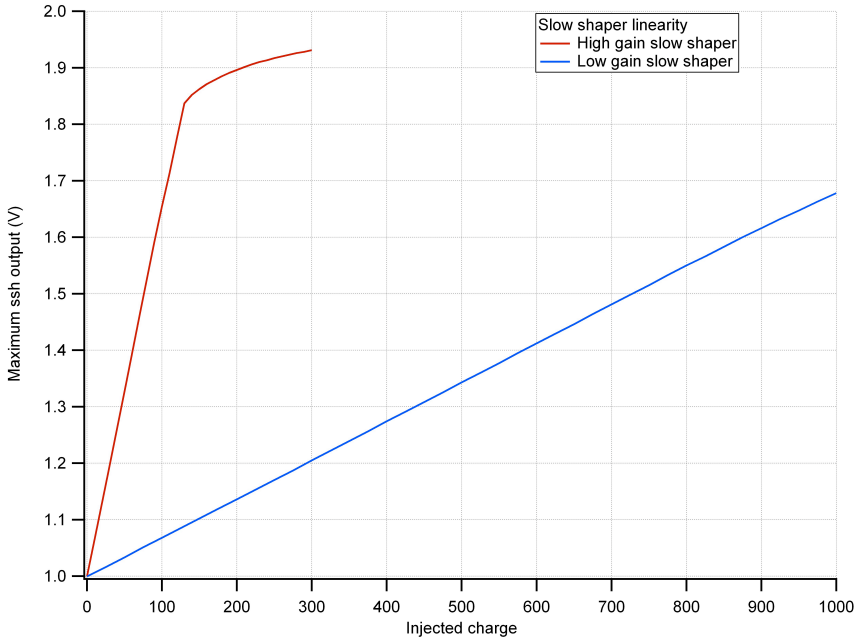

Figure 4.17. Simulated slow shaper linearity. Red curve: high gain linearity until 300 p.e.; Blue curve: low gain linearity until 1000 p.e.

The dynamic range for the two channels has been confirmed by these simulations. The high gain channel can work up to 100 p.e. with good performance better than the 0.3 % as illustrated in Figure 4.18. The low gain channel can work until important input signals (1000 p.e.) with good performance better than 1 % (Figure 4.19).

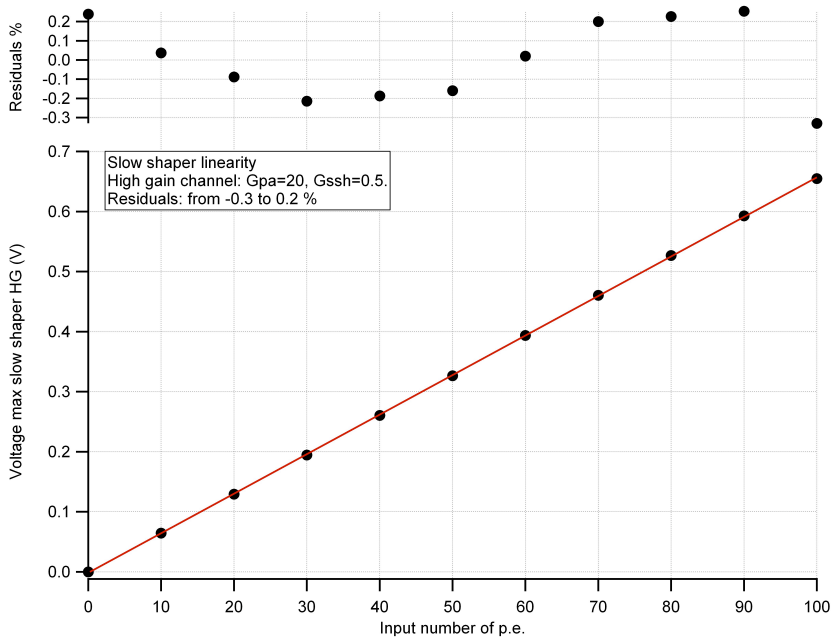

Figure 4.18. Simulated slow shaper high gain linearity for shaping time of 50 ns and gain 0.5. Residuals from -0.3 % to 0.2 %.

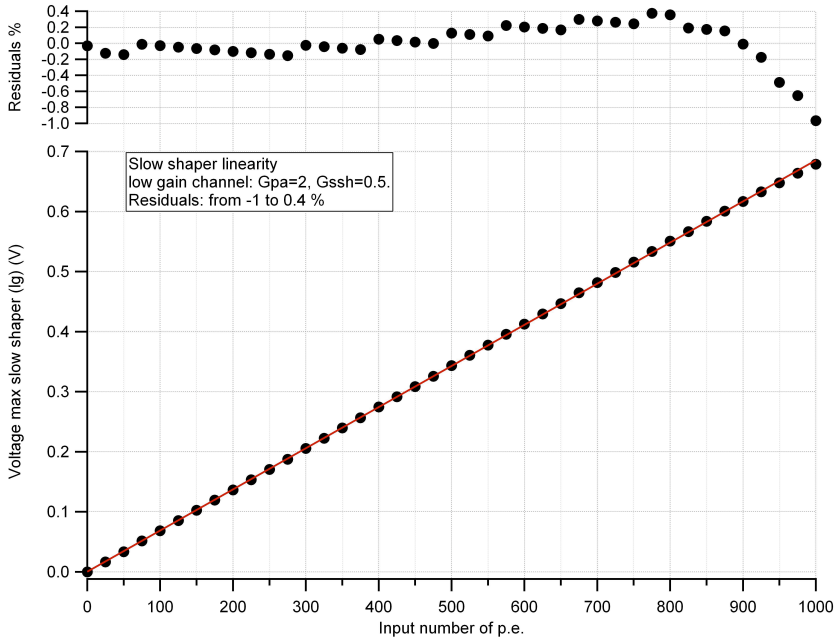

Figure 4.19. Simulated slow shaper low gain linearity for shaping time of 50 ns and gain 0.5. Residuals from -1 % to 0.4 %.

Finally the equivalent output noise has been simulated. Figure 4.20 and Figure 4.21 display the noise curves respectively for the high and low gain slow shaper for a shaping time of 50 ns and gain 0.5. The rms noise for the two shapers has been calculated at 10 MHz indicating values of 630 µV and 560 µV respectively for high and low gain.

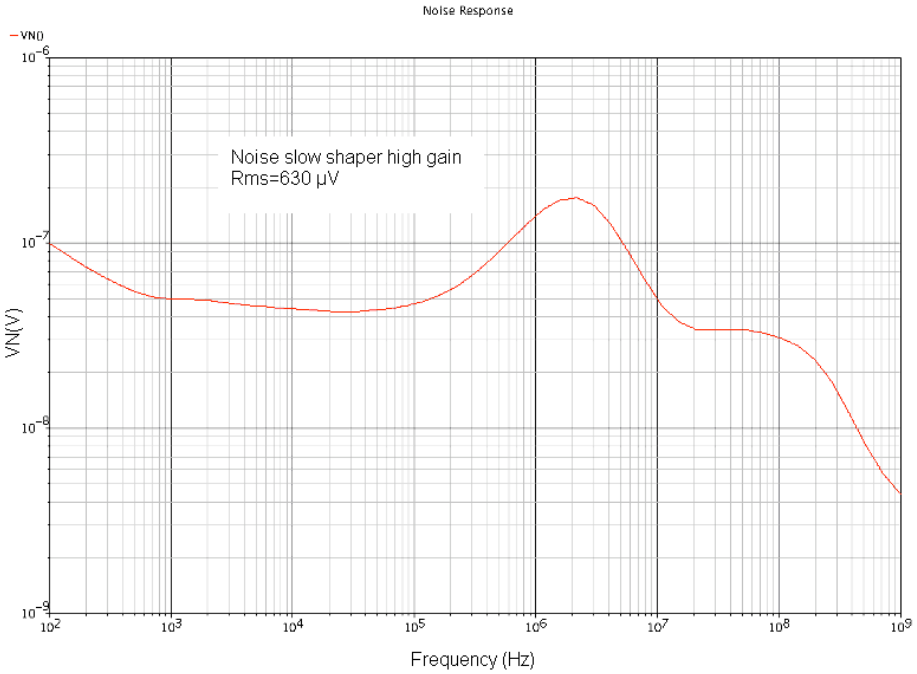

Figure 4.20. simulated slow shaper high gain equivalent output noise for shaping time of 50 ns and gain 0.5. Rms noise at 10 MHz: 630 µV.

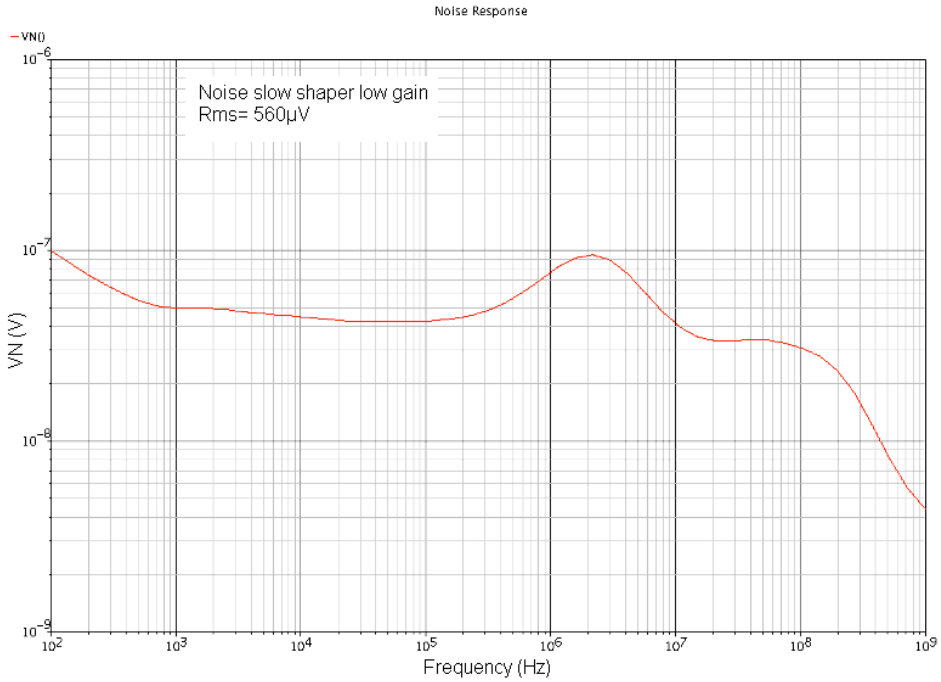

Figure 4.21. Simulated slow shaper low gain equivalent output noise for shaping time of 50 ns and gain 0.5. Rms noise at 10 MHz: 560 μV.

3.5. Dual Track & Hold

The maximum value of the slow shaper and the TDC ramp value are saved in the analog memory as in the first version.
The splitting of the channel in high and low gain components and the improvements in the TDC ramp with a new conception of the fine time measurement induce that the number of T&H are multiplied by two.
Figure 4.22 illustrates the general schematic of the SCA used to save the charge values. Two T&H cells are used to save the high gain as well as for the low gain. Each one has the same schematic as the first version as shown in Figure 4.23. An extra discriminator is added to allow the automatic gain choice. The threshold is provided by an extra DAC. The choice of the gain can be forced by slow control parameters.
Only the good charge value is digitized then by the ADC.

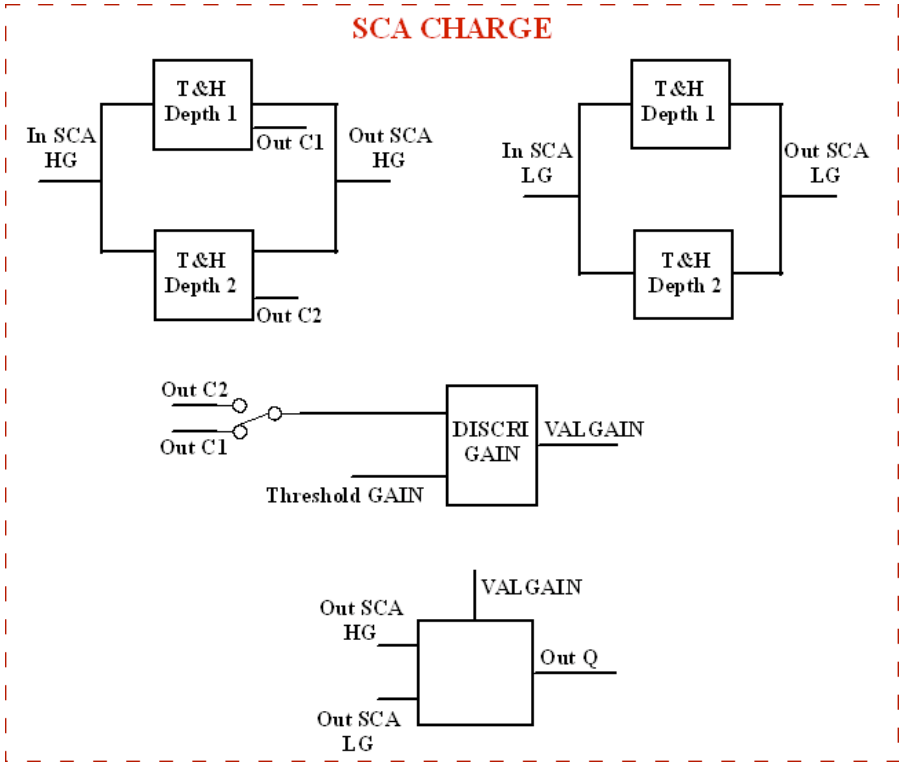

Figure 4.22. SCA Charge general schematic.

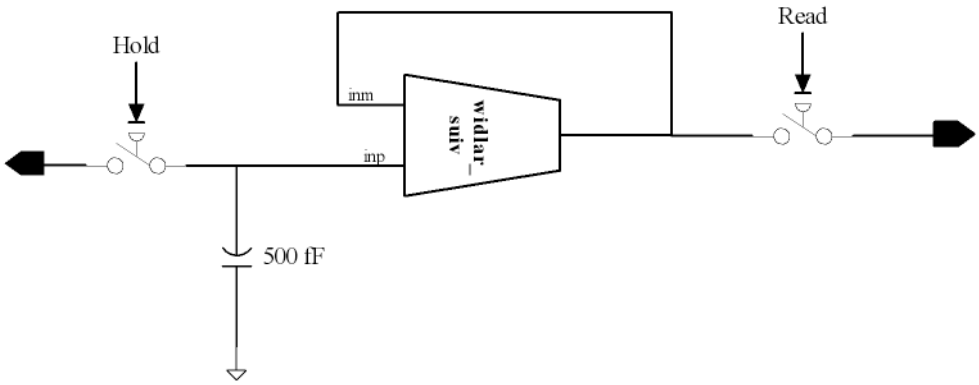

Figure 4.23. T&H cell general schematic.

Figure 4.24 illustrates the SCA for the fine time measurements, as explained in the section of the digital part. In order to avoid the dead zone observed in the measurements (§ 8 Chapter III), the values of the two ramps are saved in the T&H cells. The good time value is auto-selected by a specific module added in the SCA cell. Only the good value of the TDC ramp is then converted by the ADC.

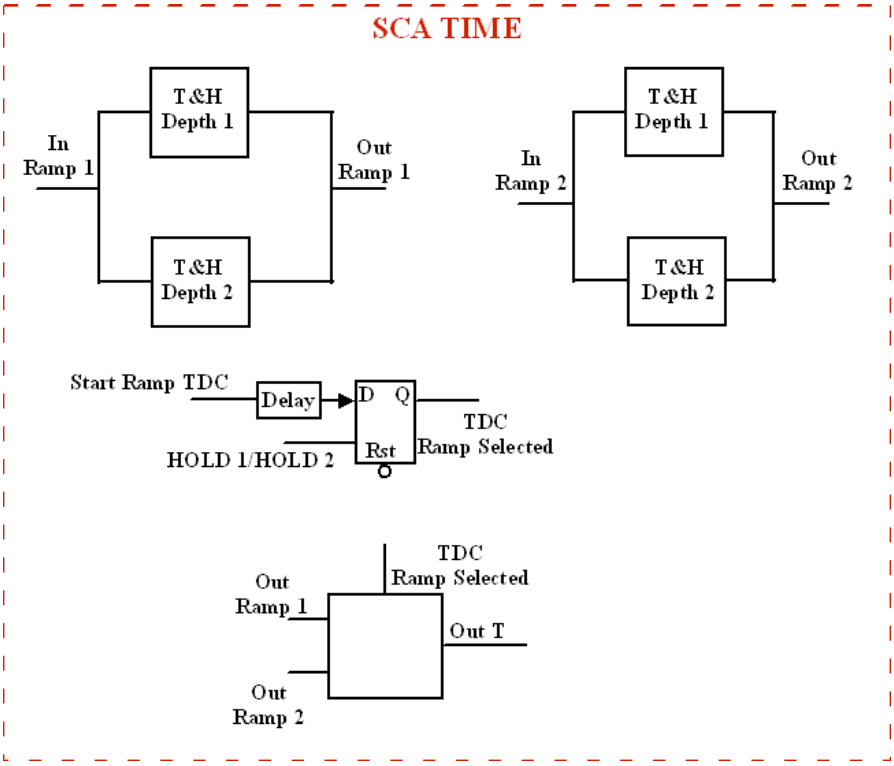

Figure 4.24. SCA time general schematic.

3.6. Layout

The numerous modifications in the schematic of the ASIC have led to a completely new layout design. New design implementation has been used to improve the noise and coupling:

- A new floorplanning to reduce noise and coupling signals;
- A new pin-out to reduce coupling;
- A new discriminator location distant from the input analog part to avoid the coupling signals.

Figure 4.25 shows the PARISROC 2 layout where are evidenced the different parts.

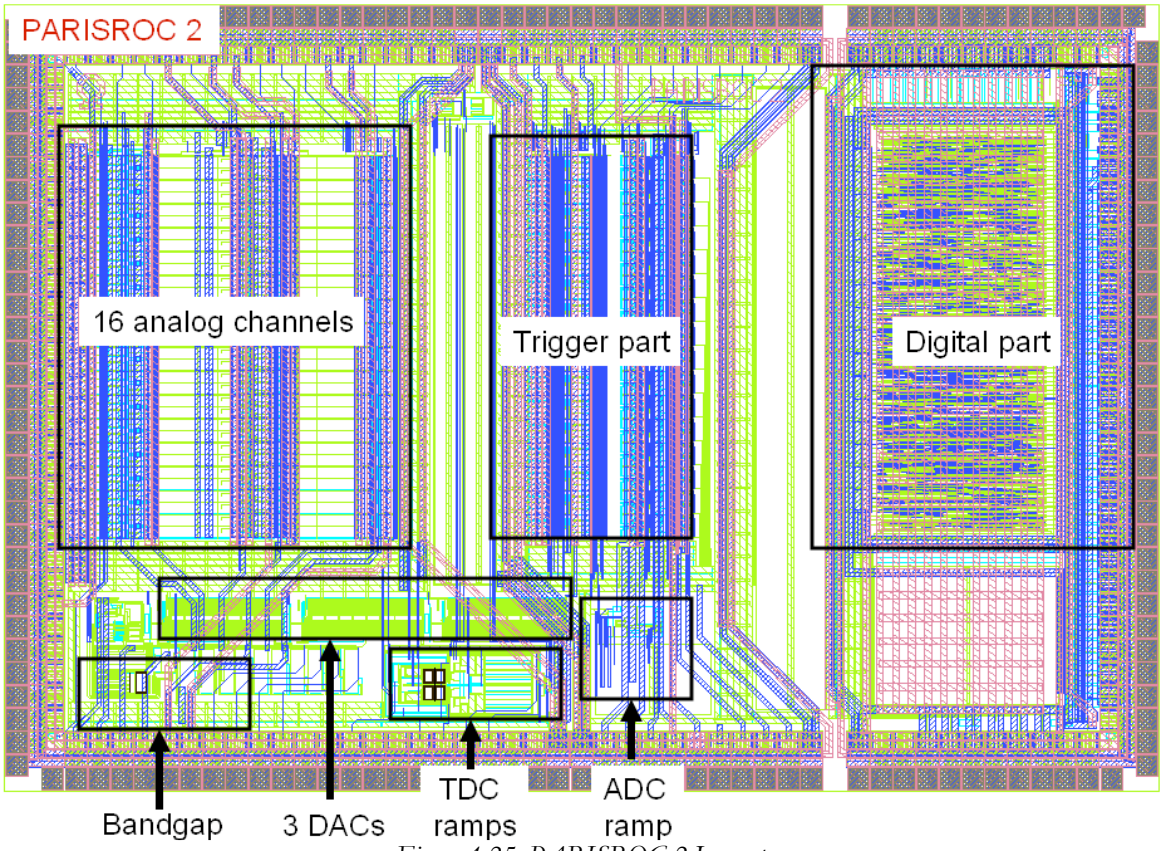

Figure 4.25. PARISROC 2 Layout.

4. Measurements

The second version of PARISROC chip was sent for fabrication in November 2009. A batch of 5 packaged ASICs and 20 dies was produced and received in February 2010.
A phase of characterization has started in March 2010 as for the first version. All the analog bocks have been tested and the preliminary analysis has shown a correct overall behavior. The main measurements will be presented in this section in order to compare the two version results and to demonstrate the improvements.
A new test board was designed because of the new chip pin-out (Annex IV) following the same conception of the first version. The same test bench has been used for the measurements and a new Labview program has been developed. This one was required by the numerous modifications bring in the second version in terms of slow control bits (Annex V), probe register (Annex VI), etc.

4.1. Analog part tests

The chip measurements start with the power dissipation (15 mW per channel), the classical pin-out dc levels and analog pedestal tests. These ones have shown good results. They have been followed by the analog output signal observation.
As for the first chip version, the same input analog signal has been used and is described in § 2.3 Chapter III.

4.1.1. Preamplifier

Figure 4.26 shows the high gain preamplifier (20) output waveform with amplitude of 12 mV for 1 p.e. injected in the input. Table 4.6 compares the performance, signal amplitude and the rms noise values, obtained in simulation and in measurement.

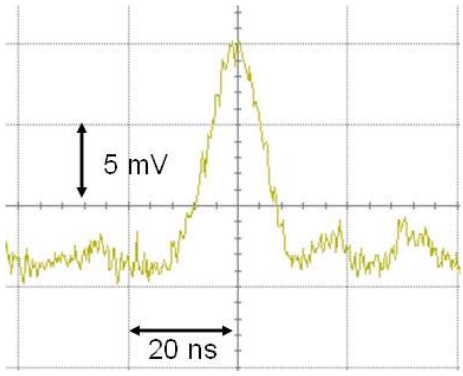

Figure 4.26. Preamplifier high gain output at 1p.e.

Preamplifier high gain	1 p.e. maximum output voltage	Noise	SNR
Measurements	12 mV	1 mV	12
Simulation	12.5 mV	610 µV	20

Table 4.6. Preamplifier high gain performances.

The measurements of PARISROC 1 indicated a noise of 1 mV and a SNR of 5. The high gain channel allows an improvement of the SNR for small signals measurements.
Table 4.7 lists the low gain preamplifier performances. The SNR for the low gain is not critical because this path is designed for high input signals (> 90 p.e.).

Preamplifier low gain	1 p.e. maximum output voltage	Noise	SNR
Measurements	1.2 mV	900 µV	1.3
Simulation	1.3 mV	~ 500 µV	~ 3

Table 4.7. Preamplifier low gain performances.

4.1.2. Slow shaper

The slow shaper output waveform is tested in the default configuration (50 ns shaping time and gain 0.5). Figure 4.27 illustrates the output signal at 1 p.e. in the input and indicates an amplitude of 6 mV.
Table 4.8 lists the results obtained in measurement and simulation. The rms noise measured is around 1 mV showing a nice improvement with respect to the 4 mV obtaining for the first version. The signal to noise ratio has also been ameliorated going from 3 for the first version to 6 for the second.

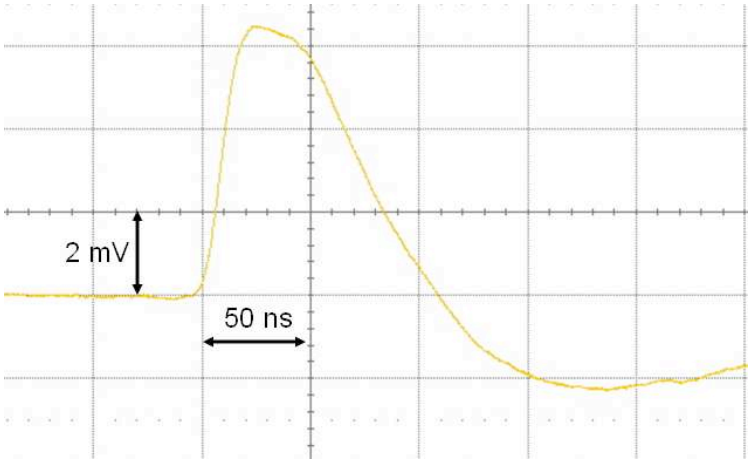

Figure 4.27. Slow shaper high gain average output at 1 p.e. Shaping time: 50 ns; slow shaper gain: 0.5.

Slow shaper high gain τ= 50 ns Gain= 0.5	1 p.e. maximum output voltage	Noise	SNR
Measurements	6 mV	1 mV	6
Simulation	6.3 mV	630 µV	10

Table 4.8. Slow shaper high gain performances.

4.1.3. Fast shaper

Finally the fast shaper output signal has been observed at 1 p.e. with amplitude of 78 mV (Figure 4.28). Table 4.9 indicates the fast shaper performances; an rms noise of 3.4 mV is measured in agreement with simulation. A difference in amplitude of 26 % has been observed such as in the first version (~ 20 %).

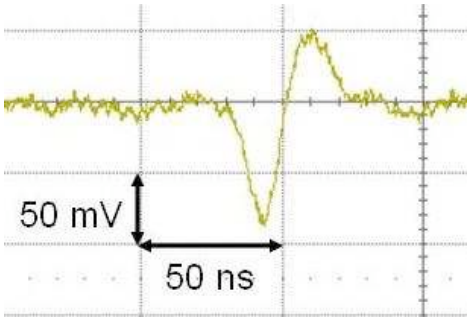

Figure 4.28. Fast shaper output at 1 p.e.

Fast shaper high gain	1 p.e. maximum output voltage	Noise	SNR
Measurements	78 mV	3.4 mV	23
Simulation	106 mV	3.4 mV	31

Table 4.9. Fast shaper performances.

4.1.4. Noise

The main problem observed in the first version of PARISROC chip was the noise. In particular the clock noise and the extra noise injected in the input capacitance switches. Therefore an important phase of investigation has been done during the design of the second version.
The design improvements studied to avoid these problems are:

- The modification of the preamplifier Cin replaced by a single value not switched;
- The modifications on the slow shaper schematic.

The measurements on PARISROC 2 have indicated that the clock noise and the extra noise are improved. Table 4.10 lists the noise performances measured on the oscilloscope. Good rms noise performance have been obtained compared to the first version measurements although with bigger values of a factor less than 2 comparing to the simulations results.

	RMS noise		
	Second version		First version
	High Gain	Low Gain	
Preamplifier	1 mV	900 µV	1 mV
Slow shaper 25ns, 16k	940 µV	880 µV	
Slow shaper 25ns, 32k	1.2 mV	990 µV	
Slow shaper 50ns, 16k	1 mV	880 µV	4 mV
Slow shaper 50ns, 32k	1.3 mV	1 mV	
Slow shaper 100ns, 16k	1.2 mV	1 mV	6 mV
Slow shaper 100ns, 32k	1.4 mV	1.1 mV	
Fast shaper	3.4 mV		2.5 mV

Table 4.10. Analog part noise performances.

4.2. Trigger efficiency

In order to investigate the trigger efficiency, S-Curve tests are performed, scanning the threshold for a fixed channel (channel one) and different injected charges. This is an important measurement that indicates the chip capability to trigger at 1/3 of p.e. which is a primary requirement of the PMm² program. Figure 4.29 shows the trigger efficiency versus the threshold (in DAC units from 750 to 885) for the different injected charges, from 0 (the pedestal at 882 UDAC) to 500 fC (3 p.e. at 768 UDAC). The 50% trigger efficiency values extracted from this measurement are plotted, in mV, versus the injected charge (Figure 4.30). The linearity is correct down to 35 fC which corresponds to 5 σ noise with σ at 7 fC. This indicates that the threshold can be set at 1/3 of p.e. as required by the project by the clock noise improvements and the trigger creation by the high path.

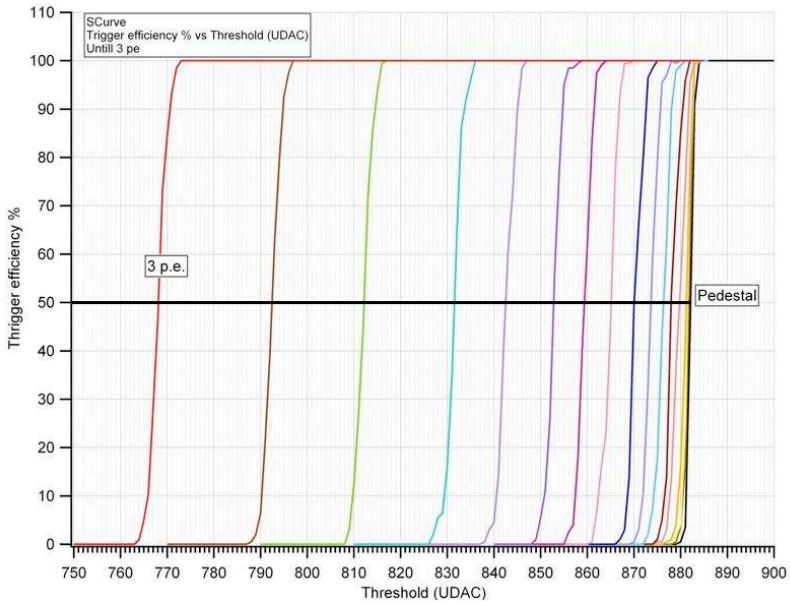

Figure 4.29. Trigger efficiency vs DAC count until 500 fC (3 p.e.).

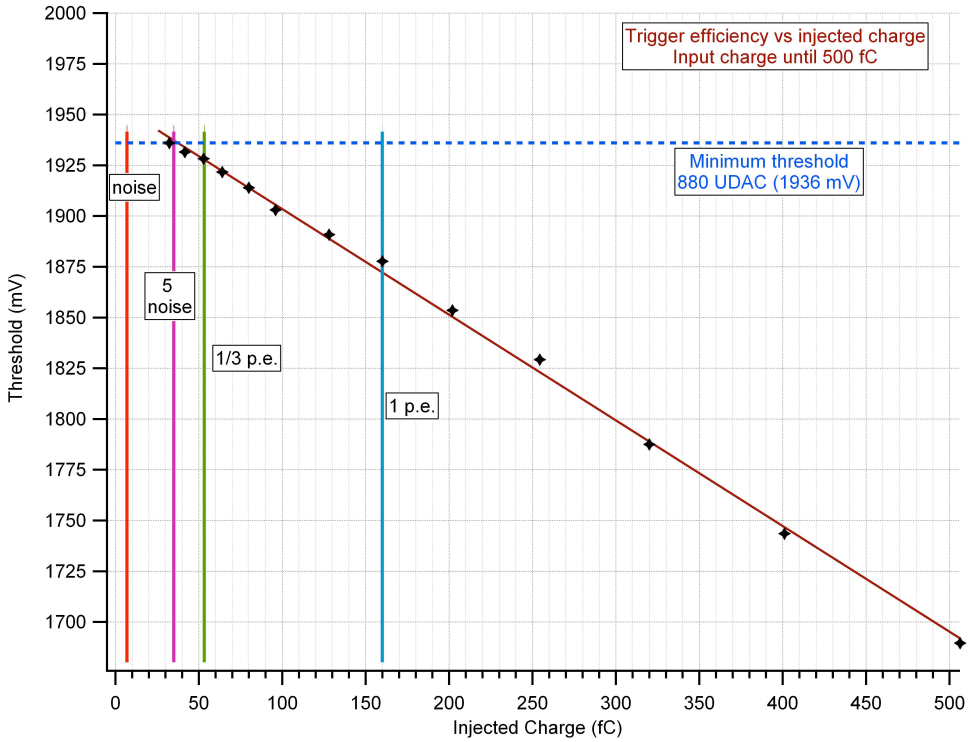

Figure 4.30. Threshold (mV) vs injected charge until 500 fC.

4.3. ADC

The ADC structure is not changed except the current of the variable current source (§ 4.6 Chapter II) used to modify the ADC number of bits.

The ADC performances have been tested with an external DC voltage (such as in PARISROC 1 test § 7.1 Chapter III). With a voltage value of 1.2 V at the 10-bit ADC (LSB=2.2 mV) input, the measurement is repeated 50000 times for each channel. Figure 4.31 shows the results obtained with the Labview program. The first plot (top left panel) represents the minimal (red), maximal (white) and means (green) values,

overall acquisitions, for each channel. In the second plot (medium left panel) there are the rms charge values versus channel number with spread around 0.1 ADC units (UADC). Finally the third plot (bottom left panel) shows an example of charge amplitude distribution for a single channel; a single value of 142 UADC is obtained.

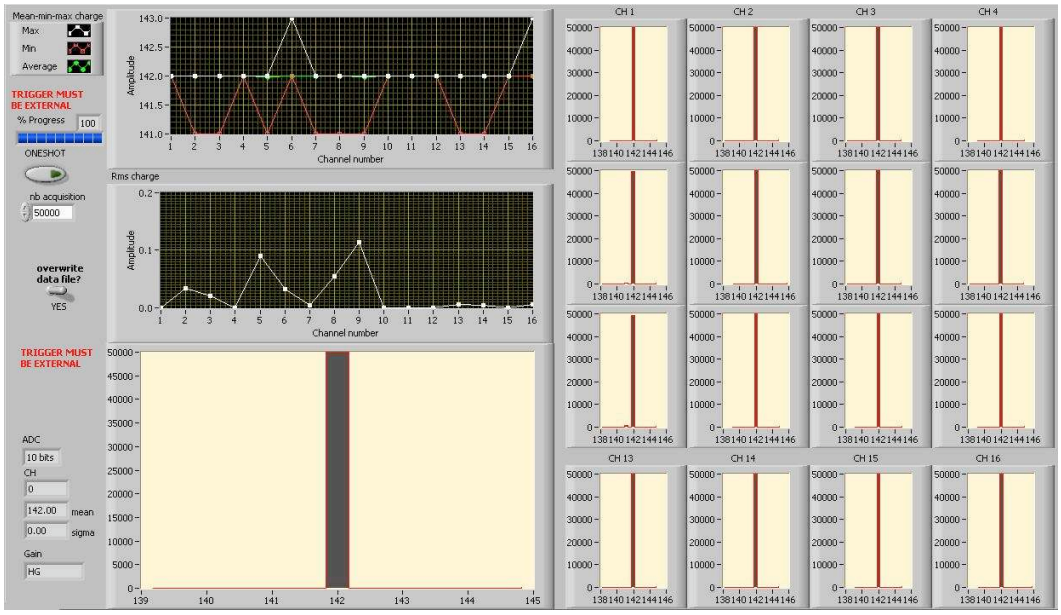

Figure 4.31. ADC performance with an external input voltage. On the left: Channels uniformity (top), rms values for all channels (medium) and single channel distribution (bottom). On the right: 16 channels distributions.

The whole chain is then tested injecting a charge in the input of the channel: the signal is amplified, auto-triggered, held in the SCA cell and converted by the ADC. This was done with the high gain channel.
With a shaping time of 50 ns and gain 0.5 the channel one charge distribution with 3 p.e. at the input is shown on the left panel of Figure 4.32. This measurement is compared with the one obtained with PARISROC 1 shown on the right panel of Figure 4.32. A σ of 2 is obtained with the second chip version that compared with 6 of the first version indicates smaller noise.
The holes of the second version that indicated the presence of the clock noise have disappeared in the second version.

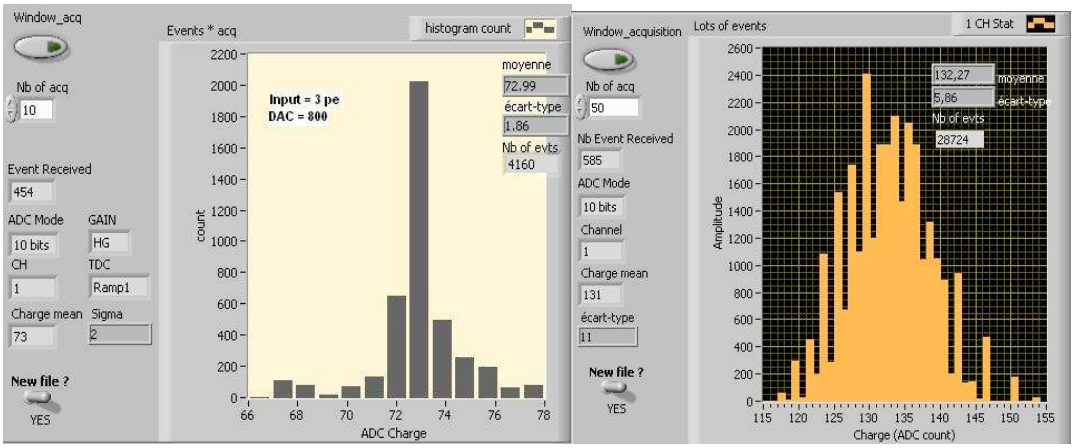

Figure 4.32. Charge distribution for channel one for 3p.e.. On the right the PARISROC 1 performances. On the left the PARISROC 2 performances.

The slow shaper linearity has been measured in order to define the dynamic range of both the high and low gain channels. It has been performed automatically by the labview program. The 10-bit ADC charge values are plotted versus the variable injected charge as shown on the following figures. The injected

signals are auto-triggered, saved in the analog memory and converted by the ADC; the whole chain is implicated in this measurement.
Figure 4.33 and Figure 4.34 represent the linearity respectively for high and low gain channel. The two plots indicate a good dynamic range until 60 p.e. with residuals better than 1 UADC for high gain and until 570 p.e. with residuals better than 1 UADC for low gain. Figure 4.35 illustrates the charge measurements for different injected charges setting the gain threshold at 60 p.e. This measurement shows the automatic gain selection that demonstrates good performance of the whole chain.
The dynamic range obtained in measurement shows smaller values than the simulation results: until 100 p.e. and 1000 p.e. respectively for high and low gain slow shaper[55].

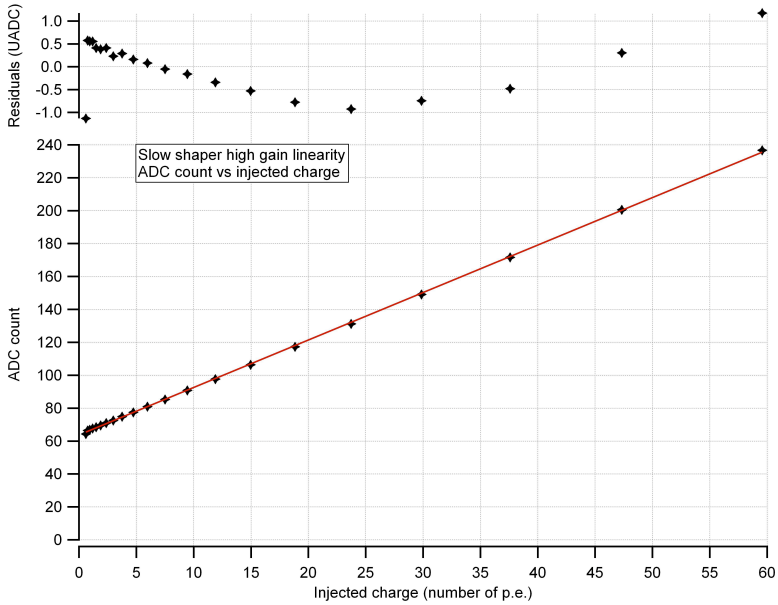

Figure 4.33. Slow shaper high gain linearity. 10-bit ADC count versus injected charge. Residuals from -1 to 1 UADC.

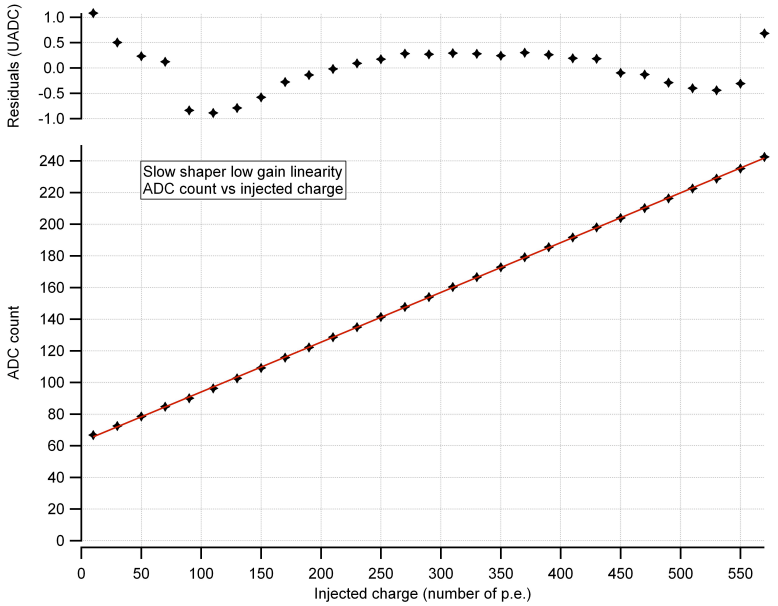

Figure 4.34. Slow shaper low gain linearity. 10-bit ADC count versus injected charge. Residuals from -1 to 1 UADC.

[55] The slow shaper linearity in simulation has been performed without load to the output.

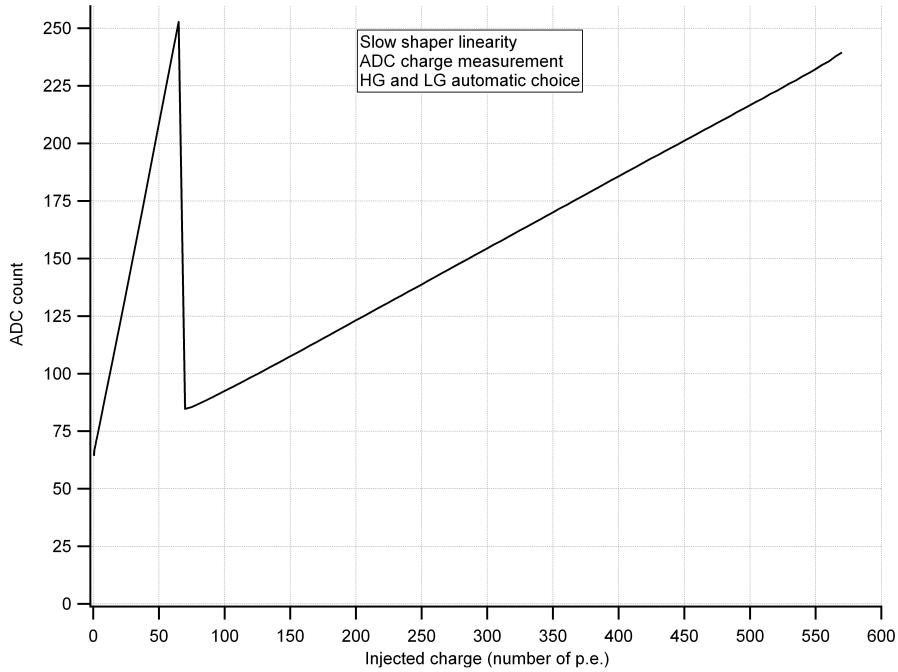

Figure 4.35. Slow shaper high and low gain linearity.

4.4. Time measurements

As explained previously the TDC ramp block has been modified to improve the ramp linearity and to eliminate the dead zone observed in measurement (§ 8 Chapter III).

The preliminary measurements (made at IPNO) will be explained in this section.
The same configuration and input signal of PARISROC 1 (explained in § 8.1 Chapter III) has been used for PARISROC 2.

The TDC ramp has been reconstructed from the time values saved in the analog memory and converted by the ADC (10-bit). The validation of the good ramp is made automatically as explained in § 3.1 Chapter IV.
The TDC ramp reconstructed is displayed in Figure 4.36. The mean time dynamic range of the two ramps is about 100 ns and the "dead zone" observed in PARISROC 1 between the two ramps (of around 30 ns) has disappeared.

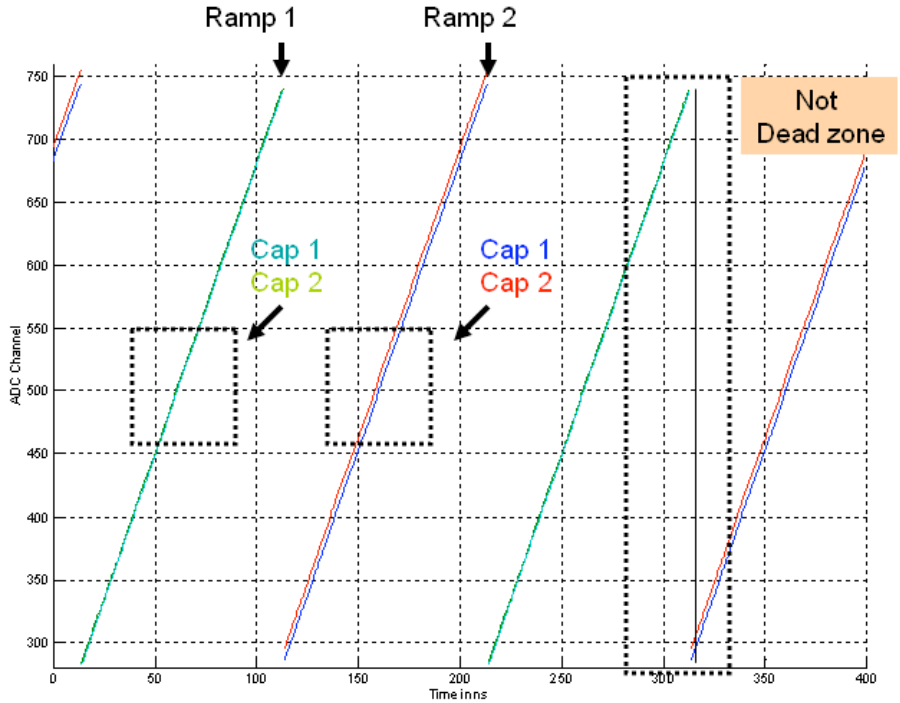

Figure 4.36. TDC ramp reconstruction by time values saved in the SCA of depth 2: capacitance C1 is the blue (pale-blue) curve and capacitance C2 the red (green) curve.

The linearity of the two ramps has been calculated considering the linear zone and Figure 4.37 illustrates the first ramp (Ramp1) linearity for the two SCA capacitances. The ramp resolution for the first (second) capacitance is of 217 ps/ UADC. The slope difference between C1 and C2 is of 0.6 UADC (128 ps). The residuals have values of ± 3.1 UADC which indicate an error of ± 674 ps. This is a systematic error which can be corrected offline.

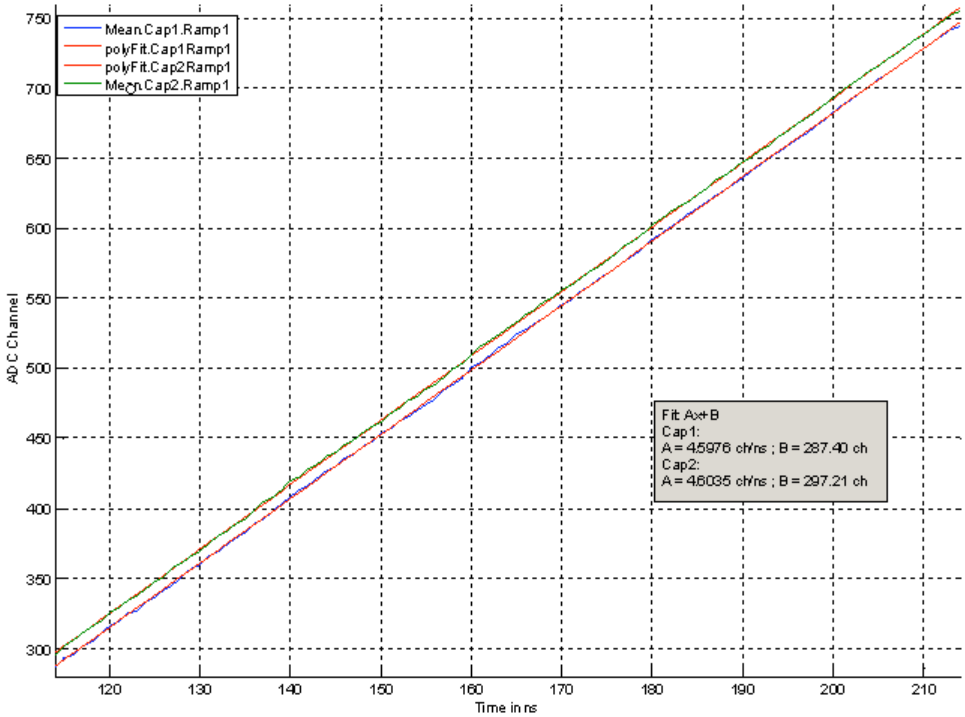

Figure 4.37. TDC ramp 1 linearity with fit. Blue: capacitance 1; Red: capacitance 2.

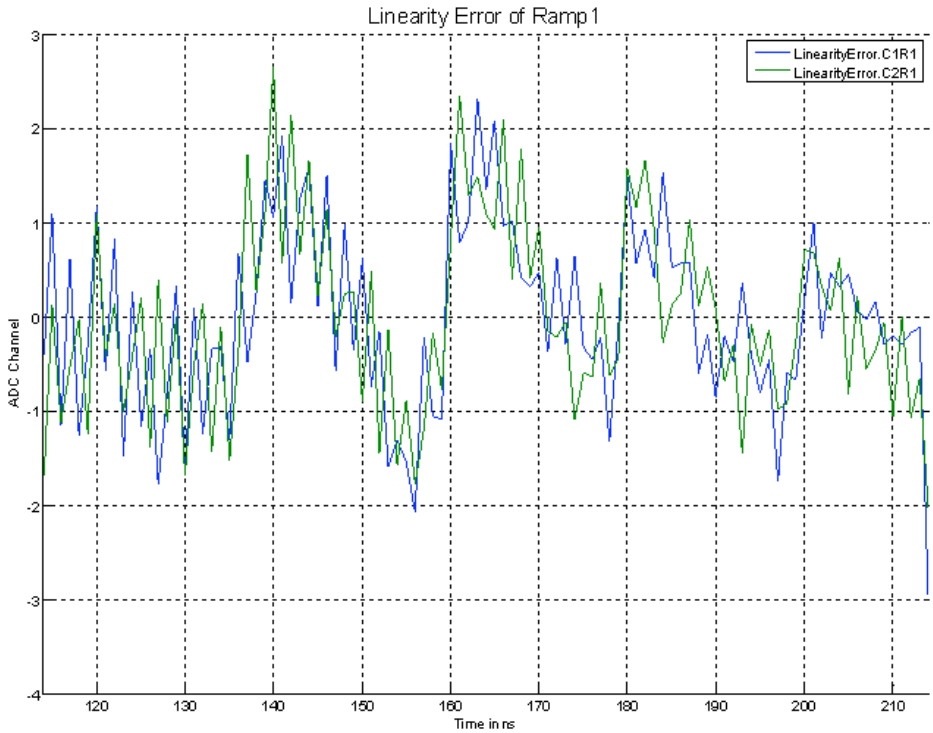

Figure 4.38. Residuals TDC ramp 1 linearity. Blue: capacitance 1; Green: capacitance 2.

The rms noise calculated for the first ramp is illustrated in Figure 4.39. The blue (red) curve indicates the rms noise values for C1 (C2) with rms value of 99 ps (102 ps) an maxim value of 322 ps (306 ps).

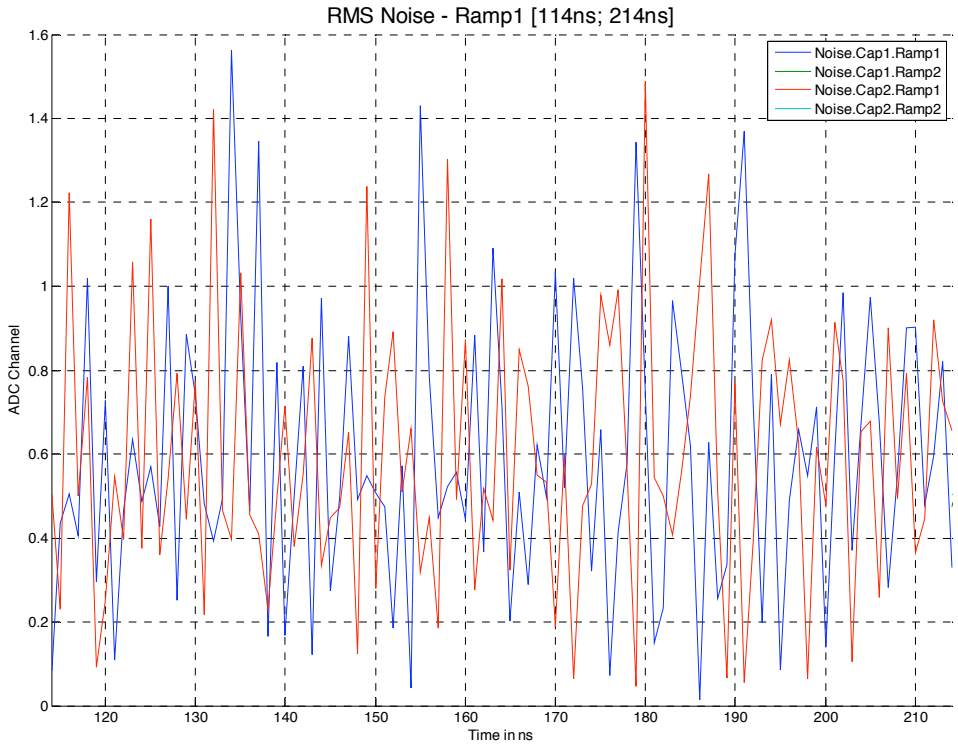

Figure 4.39. Rms noise TDC ramp 1.C1:Blue; C2: Red.

The same measurements for the ramp 2 indicate residuals with values of ± 2.5 UADC then an error of ± 519 ps. The rms noise obtained for C1 (C2) is of 111 ps (101 ps) with maximum value of 341ps (356 ps). Table 4.11 lists the ramp TDC performance of the two ASIC versions. The values indicate evident improvements in time precision and dead time obtained with the second version.

	First version	Second version
Time dynamic range	83 ns	100 ns
"dead zone"	30 ns	0
linear zone	70 ns	100 ns
Ramp 1 linearity residuals	-6 and 6.5 UADC	-3 to 3 UADC
Ramp 2 linearity residuals	-6 and 8.3 UADC	- 2.5 to 2.5 UADC
Ramp 1 error	918 ps	674 ps
Ramp 2 error	1.1 ns	519 ps

Table 4.11. PARISROC one and two TDC performances.

5. PMT measurements

With the first chip version (§ 9 Chapter III) the ASIC performance was tested with a real PMT signal. The results obtained indicated:

- The presence of the clock noise;
- A good agreement between the single p.e. spectrum measured with the chip and the oscilloscope;
- Extra sub-threshold events.

With the same set-up used previously (§ 9.1 Chapter III) the PARISROC 2 ASIC has been tested with 1-inch PMT. The preliminary tests are shown in Figure 4.40 which represents the charge measurement obtained with the whole chain of the ASIC with the 1-inch PMT at a voltage of 1200 V and gain at 10^7. The measurement has been repeated with different threshold. There is an excellent agreement between the

ADC measurements (continuous lines) and the digitizing oscilloscope (dot line) and a smaller number of events below the threshold have been observed. These measurements confirm that the clock noise has disappeared.

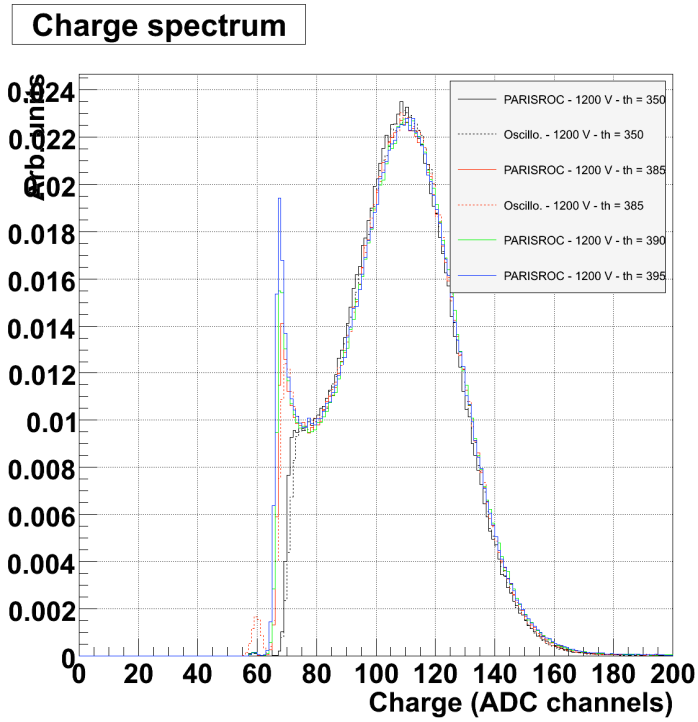

Figure 4.40. Charge histograms 1-inch PMT at a voltage of 1200 V (gain around 10^7) versus thresholds (350, 385, 390 and 395). The pedestal is at 58 ADC channels.

The PARISROC 2 tests with the PMTs are actually under investigation. The ASIC will be used with the complete project structure: the front-end, the underwater cables, the surface card and the DAQ. All this structure will be tested, in the next months, in a large demonstrator realized by the IPNO in November 2009 and mounted with the 8-inch PMTs in July 2010.

6. Conclusion

The bugs observed in the first version of the chip have been corrected in the second version, described in this chapter. The PARISROC 2 has a more complex structure then a long phase of measurements is expected. It has started in March 2010 and it is still in progress.
A first analysis of all the PARISROC 2 blocks has shown good overall performances in terms of:

- Analog signal;
- Input dynamic range;
- Noise (better clock noise);
- Trigger efficiency.

The preliminary tests on the second version show that the chip has fulfilled the requirements of the PMm² program (§ 7 Chapter I) in terms of dynamic range, trigger efficiency at 1/3 of p.e. and triggerless mode acquisition.

Conclusion

During these three years of thesis in the microelectronics group of Orsay (OMEGA), I've been involved in the development of the R&D project PMm² more especially in the design and the tests of the front-end ASIC.
The PMm² project "Innovative electronics for photo-detectors array used in high energy physics and Astroparticles", intended to perform a new generation of "smart photo-detectors" composed by sensor and readout electronics. The front end ASIC has a crucial role in this innovating concept as it evolves towards a System-On-Chip, self triggering and digitizing internally the data, turning the detector into a "smart detector".

The main specifications of this ASIC, named PARISROC (stands for "Photomultiplier ARray Integrated in SiGe Read Out Chip"), were to auto trigger on 1/3 photo electron, provide a charge measurement up to 50 pC and a time measurement better than 1ns. All the channels are handled independently by the digital part which means that only channels that have triggered are digitized and the data transferred to the internal memory and sent-out in a data driven way.
My work can be divided in 2 main phases

A. A theoretical study of the ASIC schematics through a long series of simulations and calculations that have led to the final chip design and to the realization of the first prototype PARISROC1.
   I have simulated the overall ASIC and in particular the ASIC input stage since the preamplifier is one of the most critical parts in the chip design. I performed exhaustive simulations to check the stability, the linearity and the noise of the analog part. My simulations exhibited for instance the non linearity of the preamplifier due to the variable capacitors which were therefore changed in order to reach good linearity performances.
   This simulation phase is a key point in the chip design. Each transistor size must be calculated carefully and accordingly to the required performance in particular in terms of noise and speed.

B. I also had the responsibility of the ASIC characterization. The first prototype, PARISROC1, sent for fabrication in June 2008 and received in December 2008, was tested extensively. The complexity of the ASIC has led to a long phase of test. The performance was in a good agreement with the simulations and this first version was functional in its overall behavior but tests also displayed a high clock noise and digital coupling to the inputs that prevent operation below 100 fC. Although very encouraging for a first test of a complete self-trigger-digitizer readout chain, I highlighted that three features had to be improved and integrated in PARISROC2.
   - The sensitivity need to be improved by an order of magnitude to reach the target of 1/3 photoelectron threshold. The layout has been revisited to decrease the clock noise coupling.
   - The dead time due to the conversion needed to be minimized. The simulations and calculations show that this minimization could be obtained by reducing the ADC resolution to 10 bits instead of 12 bits, reducing the conversion time by a factor of 4 to 25 µs and decreasing the dead time from 16% to 0.3%.
   - The time measurement accuracy also suffered from a dead region of 30 ns where the 2 ramps were swapped. By storing each ramp on two separate capacitors and allowing an overlap of the good regions the dead time and the time accuracy have been brought respectively to zero and to a value less than 1 ns.

I was deeply involved in the design of this second version PARISROC 2. I simulated the overall ASIC and I also designed and made the layout of analog blocks. I characterized the second prototype, received in March 2010, showing improvements with respect to the first one.

Thanks to my participation to this project PMm², that involved around 20 persons with different specialization, I have realized the importance of the design in the overall performance of huge international projects. It needs great involvement from the detector modeling to the readout architecture and implies a close collaboration between physics and mechanics groups.
The design of "System On Chip" needs a strong team of designers and I enjoyed the fruitful discussions with senior designers. I clearly improved my skills in analog design and I'm eager to continue my career in this exciting field.

Perspectives

The idea of the PMm² project to perform a new generation of "smart photo-detectors" composed by sensor and readout electronics has been demonstrated thanks to an important interdisciplinary collaboration during the three years of this R&D program.
Two demonstrators have been produced by the PMm² team; composed of a 4x4 array of photomultipliers. A first setup is equipped with 16x1-inch diameter PMTs (§ 9.5 Chapter III) and is used in the pressure vessel to verify front-end, PMTs resistence to 13 bars pressure and to validate the DAQ.
A second setup is made of 16x8-inch diameter PMTs and is used to test the full-sized mock-up of the device then to validate the mechanical design and the handling procedure. The second demonstrator has been built in November 2009 and the PMTs were mounted in July 2010.
Future tests will be performed with this demonstrator and the PARISROC 2 ASIC and it might be used by MEMPHYNO collaboration.
Figure 1 and Figure 2 illustrate respectively the schematics view and the final production of the large demonstrator.

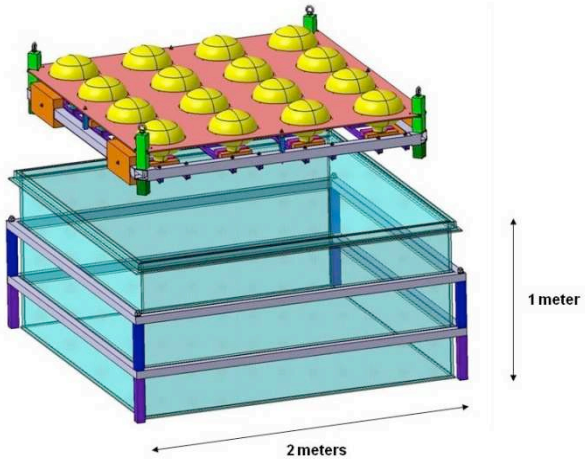

Figure 1. Scematics of the large demonstrator for testing the 16 hemispherical PMTs with the readout electronics.

Figure 2. Large demonstrator realized by the IPNO with 16 x 8-inch Hamamatsu tubes. On the right the back of the PMTs with the waterproof enclosure that contains the front-end card.

The PARISROC2 ASIC reached the requirements of the project. It is available to be used in physics experiments and tested in real detectors. Different international experiments are interested by the ASIC as the Chinese project LHAASO[56], the European MEMPHYS or LENA and LBNE in USA.
Various status reports of the ASIC[57], as well as the PMm² project, have been given at international conferences (TWEPP, IEEE NSS, TIPP, etc) during these years and numerous papers have been published in main expert reviews.

[56] The Large High Altitude Air Shower Observatory.

[57] Conforti Di Lorenzo, S. et al. (Omega/LAL), *PARISROC a Photomultiplier Array Integrated Read Out Chip*. Presented at the Nuclear Science Symposium Medical Imaging Conference, Orlando, Florida, USA, Oct 25-31, 2009. To be published in IEEE Nuclear Science Symposium Conference Record (NSS/MIC), pp. 1074-1081 (2010), Hal-00439367. ArXiv0912.1269, LAL/RT 09-25.
Conforti Di Lorenzo S. et al. (Omega/LAL), *PARISROC, a photomultiplier array integrated readout chip*. Presented at the Topical Workshop on Electronics for Particle Physics (TWEPP-09), Paris, France, Sept. 21-25, 2009. CERN-1235829.

Annex I

PARISROC 1 Slow Control Register

bits	Register description	Sub add	ASIC Register Name	Default value
16	Enable input test (channel 0 to 15)	0	test_input	no
128	Gain preamp compensation (1 pF; 0.5 pF….17 fF) (ch0…15)	16	sw_cfb <7:0>	sw_cfb<6> (0.5pF)
3	Total gain choice (4 pF; 2 pF; 1 pF)	144	sw_cin<2:0>	sw_cin<2> (4pF)
3	Slow shaper time constant (200 ns; 100 ns; 50 ns)	147	sw_rc<2:0>	sw_rc<0> (50ns)
1	Trigger input choice (0=internal; 1=external)	150	choix trig	internal
1	Trigger polarity choice (0=direct; 1=inverted)	151	polar discri	direct (positive)
32	Allow to mask discriminators (channel 0 to 15)	152	Mask (discri1 -discri2)	no
6	Delay for the ”trigger” signals (from MSB to LSB)	184	dac_delay<5:0>	dac-delay<0>
1	ADC input choice (0=internal; 1=external)	190	choix_in_adc	internal
1	discriADC polarity choice (0=direct; 1=inverted)	191	inv_discriADC	direct (positive)
64	per channel 4-bit DAC (channel 0 to 15) (from LSB to MSB)	192	dac_4bits	no
10	10-bit DAC (LSB-MSB) discri0_threshold	256	B0<0:9>	no
10	10-bit DAC (LSB-MSB) discri1_threshold	266	B1<0:9>	no
1	small dac	276		no
1	TDC delay input choice	277	extTDCdelay_cmd	internal
2	ADC precision : 12, 10 or 8 bits	278		12bits
		280		

Annex II

PARISROC 1 probe register

bits	Register description	Subadd	ASIC Register Name	Output probe
32	Slow shaper + preamplifier outputs (channel 0 to 15)	0	aprobe	analog
32	trigger delayed + not delayed outputs (channel 0 to 15)	32	probe_dig	dig2+dig1
32	4bit DAC + fast shaper outputs (channel 0 to 15)	64	probe_analog	analog
96	6 digital signals for SCA (channel 0 to 15) (note 1)	96	probe _sca	dig2+dig1 (note 1)
2	Internal start ramp 1 + 2 for TDC	192	probe_tdc	dig1+dig2
2	TDC ramp 2 +1	194	probe_tdc	analog
1	startb_ADC	196		dig1
1	start_ramp_TDC	197		dig1
		198		
(note 1) signals : sel_colb1 + col to read1 + T&H1 + sel_colb2 + T&H2 + col to read2				
output probe : dig2 + dig1 + dig1 + dig1 + dig2 + dig2				

Annex III

PARISROC 1 pin out

Pin	Pin Name	Pin Type	Description	measure PCB Chip2 V
1	NC	NC		
2	vbo_pa	Analogue Bias	preamp output stage bias (R= 20K to vdd , Ibias= 125uA)	1,257
3	srin_sc	Digital Input	data input of slow control shift register	
4	gnd_pa	Power	lowest preamp supply (I=27mA)	21,43
5	vss	Power	substrate supply (I=0mA)	
6	vdd_sca	Power	highest power supply for buffers (SCA+ output) (I=9mA)	3,27
7	vbm_pa	Analogue Bias	preamp middle stage bias (R= 100K to gnd , Ibias= 25uA)	2,064
8	vb_cf	Analogue Bias	preamp feedback bias (to vdd , Ibias= 2.5nA)	0,434
9	vbi_ota_pa	Analogue Bias	ota_preamp input stage bias (to vdd , Ibias=0. 5nA)	0,34
10	vbo_ota_pa	Analogue Bias	ota_preamp output stage bias (to gnd , Ibias= 5nA)	2,648
11	vdda_pa	Power	highest input preamp supply (very sensitive ; I=5mA)	
12	in<0>	Analogue Input	channel inputs	
13	in<1>	Analogue Input		
14	in<2>	Analogue Input		
15	in<3>	Analogue Input		
16	in<4>	Analogue Input		
17	in<5>	Analogue Input		
18	in<6>	Analogue Input		
19	in<7>	Analogue Input		
20	vdda_pa	Power	highest input preamp supply (very sensitive ; I=5mA)	3,27
21	in<8>	Analogue Input	channel inputs	
22	in<9>	Analogue Input		
23	in<10>	Analogue Input		
24	in<11>	Analogue Input		
25	in<12>	Analogue Input		
26	in<13>	Analogue Input		
27	in<14>	Analogue Input		
28	in<15>	Analogue Input		
29	vdda_pa	Power	highest input preamp supply	

			(very sensitive ; I=5mA)	
30	out_bg	Analogue Bias	Bandgap voltage output (Vbg=2.6V)	2,506
31	vbi_otabg	Analogue Bias	ota for bandgap bias (R=750K to vdd ; Ibias=3.3uA)	0,481
32	ibi_otadac	Analogue Bias	ota for dac input stage bias (R=15K to vdd ; Ibias=160uA)	0,805
33	ibo_otadac	Analogue Bias	ota for dac output stage bias (R=100K to vdd ; Ibias=25uA)	0,618
34	iref_dac	Analogue Bias	Current dac reference (R=300K to Vbg ; Iref=5uA)	0,424
35	vdd_dac	Power	highest DAC supply (I=0.75mA)	3,28
36	vss	Power	substrate supply (I=0mA)	
37	gnd_bg	Power	lowest bandgap supply	0,14
38	vref_otadac	Analogue Bias	ota for dac voltage reference=2V (50K to Vbg + 200K to gnd)	2
39	in_calib	Analogue Input	Calibration input (Voltage , Ctest =3pF per channel)	
40	vdd_bg	Power	highest bandgap supply	3,28
41	vref_pa	Analogue Bias	preamp voltage reference=1V (160K to Vbg + 100K to gnd)	0,972
42	vg_pa	Analogue Bias	grid voltage for preamp cascode=1.8V (24K toVbg+54.5K to gnd)	1,774
43	vref_ssh	Analogue Bias	1st stage of slow shaper volt. ref=1.1V (150K to Vbg+109K to gnd)	1,019
44	vref2_ssh	Analogue Bias	Slow shaper voltage reference=1V (80K to Vbg + 50.2K to gnd)	0,995
45	vref_start_ramp_tdc	Analogue Bias	TDC reference voltage =1.35V (36K to Vbg + 39K to gnd)	1,06
46	vref_fs_dummy	Analogue Bias	fast shaper dummy voltage=1.8V (24K to Vbg + 50.4K to gnd)	1,757
47	vref_fs	Analogue Bias	fast shaper voltage reference=2V (24K to Vbg + 81K to gnd)	1,94
48	gnd_dac	Power	lowest dac supply (I= 0.75mA)	2,25
49	vslope_ramp_tdc	Analogue Bias	TDC slope voltage =1.04V (30K to Vbg + 20K to gnd)	1,03
50	vslope_ramp_wiki	Analogue Bias	ADC slope voltage =1.04V (30K to Vbg + 20K to gnd)	0,569
51	vth2	Analogue Bias	Threshold voltage provided by 10bit DAC 2	
52	vth1_dac4b	Analogue Bias	Threshold voltage provided by 10bit DAC 1	
53	vb_dac4b	Analogue Bias	4bit dac bias (R=50K to vdd ; Ibias=50uA)	0,81
54	vref_start_ramp_wiki	Analogue Bias	ADC reference voltage =1.38V (36K to Vbg + 41K to gnd)	0,909
55	vss	Power	substrate supply (I=0mA)	
56	vss	Power	substrate supply (I=0mA)	
57	gnda_ramp_tdc	Power	lowest ramp tdc supply (I=30mA)	1,9
58	vb_tdc_inteamp	Analogue Bias	bias for integrator for TDC (R=15K to gnd ; Ibias=150uA)	2,092
59	in_adc_ext	Analogue Input	external input for internal adc	
60	vb_delay_tdc	Analogue Bias	bias for delay bloc for TDC (R=160K to gnd ; Ibias=15uA)	2,267
61	vdda_ramp_tdc	Power	highest ramp tdc supply (30mA)	3,28
62	ramp_ADC	Analogue Output	output of the ramp built for wilkinson ADC	
63	ramp_tdc_extdelay_in1	Digital Input	external inputs to adjust delay for TDC ramp	
64	ramp_tdc_extdelay_in2	Digital Input		
65	vdd_discriADC	Power	highest ADC discri supply (I= 2.2mA)	3,28

66	vbi_discriADC	Analogue Bias	input stage of ADC discri bias (R=100K to vdd ; Ibias=25uA)	0,778
67	vbo_discriADC	Analogue Bias	output stage of ADC discri bias (R=100K to gnd ; Ibias=25uA)	2,275
68	gnd_discriADC	Power	lowest discri for adc supply (I=2.2mA)	2,03
69	vbm_discriADC	Analogue Bias	middle stage of ADC discri bias (R=250K to gnd ; Ibias=10uA)	2,3
70	gnd_ADC	Power	lowest ramp adc supply (I=0.6mA)	0,7 m
71	ibias_ADC	Analogue Bias	bias for integrator for ADC (R=15K to gnd ; Ibias =150uA)	2,093
72	vdd_ADC	Power	Highest ramp ADC supply (I=0.6mA)	3,28
73	vss	Power	substrate supply (I=0mA)	
74	VL	Power	lowest trigger buffer supply	0
75	gndd_digital	Power	lowest digital part supply	1,2
76	valid_trigger	Digital Input	input to add external window for trigger	
77	trig_ext	Digital Input	external trigger input	
78	Enb_tristate	Digital Input	disable command for trigger output buffers	
79	CK_mux	Digital Input	Command to choice discri or multiplex. clock	
80	CMD	Digital Input	command to choice application	
81	clk_probe	Digital Input	clock for probe register	
82	clk_sc	Digital Input	clock for slow control register	
83	gndd	Power	lowest full custom digital part supply	
84	vss	Power	substrate supply (I=0mA)	
85	vddd	Power	highest full custom digital part supply	
86	rstb_delay	Digital Input	reset for delay cells	
87	srout_probe	Digital Output	probe shift register output	
88	srout_sc	Digital Output	slow control shift register output	
89	T<15>	Digital Output		
90	T<14>	Digital Output	trigger outputs	
91	T<13>	Digital Output		
92	StartSyst	Digital Input	command to start the digital part	
93	T<12>	Digital Output		
94	T<11>	Digital Output	trigger outputs	
95	rstb_num	Digital Input	reset for digital part	
96	T<10>	Digital Output		
97	T<9>	Digital Output	trigger outputs	
98	T<8>	Digital Output		
99	T<7>	Digital Output		
100	ClkAcqt-	LVDS Input	acquisition clock	
101	ClkAcqt+	LVDS Input		
102	ClkTS+	LVDS Input	Data transmission clock	
103	ClkTS-	LVDS Input		
104	T<6>	Digital Output	trigger outputs	
105	T<5>	Digital Output		
106	OutSerie	Digital Output	digital data output	
107	T<4>	Digital Output	trigger outputs	
108	T<3>	Digital Output		
109	TransmitOn	Digital output	output signal for data sending	
110	T<2>	Digital Output		
111	T<1>	Digital Output	trigger outputs	
112	T<0>	Digital Output		
113	RazExtCmptTsb	Digital Input	RAZ for ADC counter	
114	A<3>	Digital Input	MSB for address demux	

115	gndd	Power	lowest full custom digital part supply	
116	vss	Power	substrate supply (I=0mA)	
117	vddd	Power	highest full custom digital part supply	
118	rstb_snemo	Digital Input	reset for SNEMO use	
119	A<2>	Digital Input	3 LSB for address demux	
120	A<1>	Digital Input		
121	A<0>	Digital Input		
122	out_digprobe1	Digital output	digital probe outputs	
123	out_digprobe2	Digital Output		
124	rstb_probe	Digital Input	reset for probe register	
125	srin_probe	Digital Input	probe shift register input	
126	rstb_sc	Digital Input	reset for slow control register	
127	nor16	Digital Output	"nor" of the 16 triggers (disri0) output	
128	nor16bis	Digital Output	"nor" of the 16 triggers (disri1) output	
129	VH	Power	highest trigger buffer supply	3,28
130	vddd_digital	Power	highest digital part supply	3,28
131	vss	Power	substrate supply (I=0mA)	
132	vbo_discri	Analogue Bias	discri output stage bias (R= 200K to gnd , Ibias= 13uA)	2,514
133	gnd_discri	Power	lowest discri power supply (I=1.3mA)	1,3
134	vbi_discri	Analogue Bias	discri input stage bias (R= 100K to Vdd , Ibias= 25uA)	0,776
135	vdd_discri	Power	highest discri power supply (I=1.3mA)	3,28
136	vbm_discri	Analogue Bias	discri middle stage bias (R= 100K to gnd , Ibias= 25uA)	2,304
137	vdda_delay	Power	highest delay cell power supply (Imax =1mA)	3,28
138	vb_delay	Analogue Bias	delay cell bias (R=200K to gnd ; Ibias=10uA)	1,86
139	gnda_delay	Power	lowest delay cell power supply (Imax =1mA)	0
140	vss	Power	substrate supply (I=0mA)	
141	vss	Power	substrate supply (I=0mA)	
142	out_ota_probe_analog	Analogue Output	analog probe output (for debugging only)	
143	vb_Iss_ota	Analogue Bias	analog output buffer first bias (R=20K to Vdd, Ibias=120uA)	0,839
144	vb_buffer_ota	Analogue Bias	analog output buffer 2nd bias (R=20K to Vdd, Ibias=120uA)	0,84
145	vb_sca	Analogue Bias	buffer of the SCA bias (R= 125K to Vdd , Ibias= 20uA)	1,26
146	gnd_sca	Power	lowest power supply for buffers (SCA+output) (I=9mA)	11
147	gnd_capa_sca	Power	ground reference for the SCA capacitances (0mA)	0
148	Read	Digital Input	external "read" command input	
149	out_otaQ	Analogue Output	multiplexed analog charge output	
150	vbi_fs	Analogue Bias	fast shaper input stage bias (R= 60K to Vdd , Ibias= 40uA)	0,621
151	vbo_fs	Analogue Bias	fast shaper output stage bias (R= 60K to Vdd , Ibias= 40uA)	0,942
152	gnd_fs	Power	lower fast shaper supply (3.7mA)	7,4
153	vdd_fs	Power	highest fast shaper supply (I=3.7mA)	3,27
154	vdd_ssh	Power	highest slow shaper supply (I=17.4mA)	3,27
155	vbo_ssh	Analogue Bias	slow shaper output stage bias (R= 100K to Vdd , Ibias= 24uA)	0,984
156	vbi_ssh	Analogue Bias	slow shaper input stage bias (R= 100K to Vdd , Ibias= 24uA)	0,734
157	gnd_ssh	Power	lowest slow shaper supply (I=17.4mA)	13
158	vb_ssh	Analogue Bias	OTA slow shaper bias	1,14

			(R= 100K to Vdd , Ibias= 24uA)	
159	vdd_pa	Power	highest preamp supply (I=12mA)	3,27
160	vbi_pa	Analogue Bias	preamp input stage bias (R= 2.5K to Vdd , Ibias= 1mA)	1,388

Annex IV

PARISROC 2 pin out

Pin	Pin Name	Pin Type	Description	Measur. PCB Chip2 V
1	NC	NC		
2	Ib_otaQ	Analogue Bias	output OTAs bias (R=21K to Vdd : Ibias=120uA)	0.9V
3	in_calib	Analogue Input	Calibration input (Voltage , Ctest =1pF per channel)	
4	gnd_pa	Power	lowest preamp supply (I=57mA)	
5	vss	Power	substrate supply (I=0mA)	
6	vdd_pa	Power	highest preamp supply (I=12.5mA)	3.23V
7	ib_ota_pa	Analogue Bias	ota_preamp bias (250K to vdd , Ibias=10mA)	0.708V
8	ibm_pa	Analogue Bias	preamp middle stage bias (R= 100K to gnd , Ibias= 25uA)	1.99V
9	ibo_pa	Analogue Bias	preamp output stage bias (R= 20K to vdd , Ibias= 125uA)	1.27
10	ibi_pa	Analogue Bias	preamp input stage bias (R= 2.5K to Vdd , Ibias= 1mA)	1.41V
11	vdda_pa	Power	highest input preamp supply (very sensitive ; I=10mA)	
12	in<0>	Analogue Input	channel inputs	
13	in<1>	Analogue Input		
14	in<2>	Analogue Input		
15	in<3>	Analogue Input		
16	in<4>	Analogue Input		
17	in<5>	Analogue Input		
18	in<6>	Analogue Input		
19	in<7>	Analogue Input		
20	vdda_pa	Power	highest input preamp supply (very sensitive ; I=10mA)	
21	in<8>	Analogue Input	channel inputs	
22	in<9>	Analogue Input		
23	in<10>	Analogue Input		
24	in<11>	Analogue Input		
25	in<12>	Analogue Input		

26	in<13>	Analogue Input		
27	in<14>	Analogue Input		
28	in<15>	Analogue Input		
29	vdda_pa	Power	highest input preamp supply (very sensitive ; I=10mA)	
30	ibo_dac	Analogue Bias	DAC output stage bias (R= 100K to Vdd , Ibias= 25uA)	0.610V
31	ibi2_dac	Analogue Bias	DAC middle stage bias (R= 25K to Vdd , Ibias= 100uA)	0.737V
32	ibi1_dac	Analogue Bias	DAC input stage bias (R= 1M to Vdd , Ibias= 2,5uA)	0.501V
33	iref_dac	Analogue Bias	DAC current reference	1.892V
34	vref_dac	Analogue Bias	DAC voltage reference	1.847V
35	ib_bg	Analogue Bias	OTA bandgap bias (R= 500K to Vdd , Ibias=5uA)	0.5V
36	vdd_pa	Power	highest preamp supply (I=12.5mA)	
37	vss	Power	substrate supply (I=0mA)	
38	gnd_bg	Power	lowest bandgap supply	
39	gnd_dac	Power	lowest DAC supply (I=0.4mA)	
40	vdd_dac	Power	highest DAC supply (I=0.4mA)	3.38V
41	NC	NC		
42	vdd_bg	Power	highest bandgap supply	3.38V
43	v_bg	Analogue Bias	Bandgap voltage	2.52V
44	vref2_ssh	Analogue Bias	slow shaper 2nd stage volt. ref =1V (80K to Vbg + 53K to gnd)	1.018V
45	vref_fs	Analogue Bias	fast shaper volt. ref =1.94V (24K to Vbg +81K to gnd)	1.885V
46	vref_adc	Analogue Bias	ADC ref voltage =0.9V (36K to Vbg + 20K to gnd)	0.877V
47	vslope_adc	Analogue Bias	ADC slope voltage =0.55V (39K to Vbg + 11K to gnd)	0.565V
48	vref_tac	Analogue Bias	TDC ref voltage =1.3V (36K to Vbg + 39K to gnd)	1.327V
49	vslope_tac	Analogue Bias	TDC slope voltage =1V (30K to Vbg + 20K to gnd)	1V
50	ib_tdc1	Analogue Bias	ramp tdc ampli input stage bias (2K to gnd; Ibias=1.25mA)	1.365V
51	ib_tdc2	Analogue Bias	ramp tdc ampli output stage bias (2K to gnd; Ibias=1.25mA)	1.367V
52	vb_delay_tdc	Analogue Bias	delay cell for tdc ramp bias (R=160K to gnd ; Ibias=15uA)	2.36V
53	ib_adc	Analogue Bias	ramp adc ampli bias (15K to gnd; Ibias=160uA)	2.17V
54	ramp_ADC	Analogue Output	output of the ramp built for wilkinson ADC	
55	gnd_tdc1	Power	lowest ramp1 tdc supply (I=0.5mA)	
56	gnd_tdc2	Power	lowest ramp2 tdc supply (I=0.5mA)	
57	vdd_tdc1	Power	highest ramp1 tdc supply (I=0.5mA)	3.33V
58	vdd_tdc2	Power	highest ramp2 tdc supply (I=0.5mA)	3.33V
59	vdd_ADC	Power	Highest ramp ADC supply	3.38V

			(I=0.6mA)	
60	gnd_ADC	Power	lowest ramp adc supply (I=0.6mA)	
61	vss	Power	substrate supply (I=0mA)	
62	vss	Power	substrate supply (I=0mA)	
63	gnd_discri	Power	lowest discri power supply (I=2mA)	
64	gnd_discriADC	Power	lowest discri for adc supply (I=2.9mA)	
65	gnd_delay	Power	lowest delay cell supply (Imax=1.6mA ; Idef = 0.2mA)	
66	vdd_delay	Power	highest delay cell supply (Imax =1.6mA; Idef=0.2mA)	3.38V
67	vdd_discri	Power	highest discri power supply (I=2mA)	3.36V
68	vdd_discriADC	Power	highest ADC discri supply (I= 2.9mA)	3.36V
69	vth1	Analogue Bias	discri0 threshold provided by 10bit DAC0	
70	vth2	Analogue Bias	discri1 threshold provided by 10bit DAC1	
71	vth_gain	Analogue Bias	gain choice threshold provided by 10bit DAC2	
72	vss	Power	substrate supply (I=0mA)	
73	vss	Power	substrate supply (I=0mA)	
74	gndd1	Power	lowest full custom digital part supply	
75	vddd1	Power	highest full custom digital part supply	3.33V
76	srin_sc	Digital Input	slow control shift register input	
77	clk_sc	Digital Input	clock for slow control register	
78	rstb_sc	Digital Input	reset for slow control register	
79	srout_sc	Digital Output	slow control shift register output	
80	valid_trigger	Digital Input	input to add external window for trigger	
81	trig_ext	Digital Input	external trigger input	
82	rstb	Digital Input	reset for digital part	
83	StartSyst	Digital Input	command to start the digital part	
84	gndd2	Power	lowest digital part supply	
85	vss	Power	substrate supply (I=0mA)	
86	vddd2	Power	highest digital part supply	3.33V
87	VH	Power	highest trigger buffer supply	
88	VL	Power	lowest trigger buffer supply	
89	T<0>	Digital Output	trigger outputs	
90	T<1>	Digital Output		
91	T<2>	Digital Output		
92	T<3>	Digital Output		
93	T<4>	Digital Output		
94	T<5>	Digital Output		
95	T<6>	Digital Output		
96	T<7>	Digital Output		
97	T<8>	Digital Output		
98	T<9>	Digital Output		
99	T<10>	Digital Output		
100	T<11>	Digital Output		
101	vss	Power	substrate supply (I=0mA)	

102	T<12>	Digital Output	trigger outputs	
103	T<13>	Digital Output		
104	T<14>	Digital Output		
105	T<15>	Digital Output		
106	or16	Digital Output	"or" of the 16 triggers (disri0) output	
107	or16a	Digital Output	"or" of the 16 triggers (disri1) output	
108	d_out	Digital Output	digital data output	
109	TransmitOn	Digital output	output signal for data sending	
110	VL	Power	lowest trigger buffer supply	
111	VH	Power	highest trigger buffer supply	
112	ck_10p	LVDS Input	Data transmission clock (10MHz)	
113	ck_10n	LVDS Input		
114	ck_40p	LVDS Input	acquisition clock (40MHz)	
115	ck_40n	LVDS Input		
116	gndd2	Power	lowest digital part supply	
117	vss	Power	substrate supply (I=0mA)	
118	vddd2	Power	highest digital part supply	
119	RazExt	Digital Input	RAZ for ADC counter	
120	pwr_on	Digital Input	power pulsing command	
121	out_digprobe2	Digital Output	digital probe outputs	
122	out_digprobe1	Digital output		
123	srout_probe	Digital Output	probe shift register output	
124	rstb_probe	Digital Input	reset for probe register	
125	clk_probe	Digital Input	clock for probe register	
126	srin_probe	Digital Input	probe shift register input	
127	vdd_sc	Power	highest slow control supply	3.33V
128	gnd_sc	Power	lowest slow control supply	
129	vss	Power	substrate supply (I=0mA)	
130	vss	Power	substrate supply (I=0mA)	
131	ibo_discri	Analogue Bias	discri output stage bias (R= 200K to gnd , Ibias= 13uA)	2.57V
132	ibi_discri	Analogue Bias	discri input stage bias (R= 100K to Vdd , Ibias= 25uA)	0.780V
133	ibm_discri	Analogue Bias	discri middle stage bias (R= 100K to gnd , Ibias= 25uA)	2.36V
134	vb_delay	Analogue Bias	delay cell bias (R=100K to gnd ; Ibias=25uA)	2.28V
135	ibo_discriADC	Analogue Bias	discri ADC output stage bias (100K to gnd, Ibias=25uA)	2.3V
136	ibm_discriADC	Analogue Bias	discri ADC middle stage bias (250K to gnd, Ibias=10uA)	2.3V
137	ibi_discriADC	Analogue Bias	discri ADC input stage bias (100K to vdd, Ibias=25uA)	0.783V
138	in_adc_ext	Analogue Input	external input for internal adc	
139	ib_w	Analogue Bias	buffer of the SCA and TAC bias (R= 125K to Vdd , Ibias= 20uA)	0.838V
140	vdd_sca	Power	highest power supply for buffers (sca+tac) (I=2.6mA)	3.36V
141	gnd_capa_tac	Power	ground reference for the tac capacitances (I=0mA)	
142	gnd_sca	Power	lowest power supply for buffers (sca+tac) (I=2.6mA)	
143	gnd_capa_sca	Power	ground reference for the SCA capacitances	

			(I=0mA)	
144	vss	Power	substrate supply (I=0mA)	
145	vss	Power	substrate supply (I=0mA)	
146	out_probe_analog	Analogue Output	analog probe output (for debugging only)	
147	en_otaQ	Digital Input	disable command for charge output buffer	
148	out_otaQ	Analogue Output	multiplexed analog charge and time value output	
149	ibi_fs	Analogue Bias	fast shaper input stage bias (R= 60K to Vdd , Ibias= 40uA)	0.77V
150	gnd_fs	Power	lower fast shaper supply (I=3.85mA)	
151	vdd_fs	Power	highest fast shaper supply (I=3.85mA)	3.34V
152	ibo_fs	Analogue Bias	fast shaper output stage bias (R= 60K to Vdd , Ibias= 40uA)	0.766V
153	ibo_ssh	Analogue Bias	slow shaper output stage bias (R= 250K to Vdd , Ibias= 10uA)	0.720V
154	ibi_ssh	Analogue Bias	slow shaper input stage bias (R= 250K to Vdd , Ibias= 10uA)	0.716V
155	vdd_ssh	Power	highest slow shaper and OTAs supply (I=26mA)	3.14V
156	gnd_ssh	Power	lowest slow shaper and OTAs supply (I=26mA)	
157	vb_ssh	Analogue Bias	OTA slow shaper bias (R= 250K to Vdd , Ibias= 10uA)	0.731V
158	vref_ssh	Analogue Bias	slow shaper 1st stage volt. ref : depends on g<1:0> command	0.993V
159	vref_pa	Analogue Bias	preamp voltage reference=1V (80K to Vbg + 52.5K to gnd)	1V
160	vg_pa	Analogue Bias	grid voltage for preamp cascode=1.8V (24K toVbg+60K to gnd)	1.8V

Annex V

PARISROC 2 Slow Control Register

bits	Register description	Sub add	ASIC Register Name	default value
32	Enable input test lg +hg (channel 0 to 15)	0	test_input	no
128	Gain preamp compensation (1pF;0.5pF,0.25pF….8fF)(ch0…15) : sw_cfb<7> to sw_cfb<0> for ch0 + sw_cfb<7> to sw_cfb<0> for ch1 + …. + sw_cfb<7> to sw_cfb<0> for ch15	32	sw_cfb <7:0>	sw_cfb<5> (0.25pF) ch0 to 15
4	Preamp power pulsing : sw_pa_lg + en_pa_lg + sw_pa_hg+en_pa_hg	160		everything on
3	Slow shaper time constant (100ns; 50ns;25ns): sw_rc<2>+sw_rc<1>+sw_rc<0>	164	sw_rc<2:0>	sw_rc<1> (50ns)
2	Slow shaper gain : Rf=16K(11); 32K(01) ; 64K(00)	167	sw_g<1:0>	everything on (16K)
4	Slow shaper power pulsing : sw_ssh_lg + en_ssh_hg + sw_ssh_lg+en_ssh_lg	169		everything on
2	Fast shaper power pulsing : sw_fsh + en_fsh	173		everything on
3	otas power pulsing : en_ota_probe+en_otaQ + sw_otas	175		everything on
2	SCA power pulsing : sw_sca + en_sca	178		everything on
2	TAC power pulsing : sw_tac + en_tac	180		everything on
2	gain choice (0:normal,1:manual) and force in manual (0: HG;1:LG)	182		everything off--> normal
2	ramp choice (0:normal,1:manual) and force in manual (0: ramp1;1:ramp2)	184		everything off--> normal
1	ADC input choice (0=internal; 1=external)	186	in_adc_choice	internal

2	ADC discri power pulsing : sw_discriADC + en_discriADC	187		everything on
1	discriADC polarity choice (0=direct; 1=inverted)	189	inv_discriADC	direct (positive)
3	discris power pulsing : sw_discris + en_discri0and1 +en_gaindiscri	190		everything on
1	trigger output choice (0=discri0; 1=discri1)	193	ck_mux	discri0
1	trigger input choice (0=internal; 1=external)	194	choix trig	internal
1	trigger polarity choice (0=direct; 1=inverted)	195	polar discri	direct (positive)
6	Delay for the ”trigger” signals (from MSB to LSB) : dac_delay<5>+dac_delay<4>+…+dac_ delay<0>	196	dac_delay<5:0>	dac-delay<3>
4	disable output buffers for OR,triggers,CK40MHz,CK10MHz	202	enb_or;enb_trig;en _ck40;en_CK10	everything on
32	Allows to mask discriminators (channel 0 to 15) : D0ch0+D1ch0+D0ch1+D1ch1+ …. + D0ch15+D1ch15	206	Mask (discri0 - discri1)	no
2	reduce ADC precision : switch to 9bits + switch to 8bits	238		10bits (no switch)
2	ramp TDC power pulsing : sw_integTDC + en_integTDC	240		everything on
2	Bandgap power pulsing : sw_BG + en_BG	242		everything on
4	DACs power pulsing : en_dac0+en_dac1+en_dac2+sw_dacs	244		everything on
10	10-bit DAC (MSB-LSB) discriGain_threshold B0<0>+B0<1>+ …+ B0<9>	248	B0<0:9>	no
10	10-bit DAC (MSB-LSB) discri0_threshold B1<0>+B1<1>+ …+ B1<9>	258	B1<0:9>	no
10	10-bit DAC (MSB-LSB) discri1_threshold B2<0>+B2<1>+ …+ B2<9>	268	B2<0:9>	no
		278		

Annex VI

PARISROC 2 probe register

bits	Register description	Sub add	ASIC Register Name	output probe
16	Read SCA register to read charge output	0	Read_SCA	out _OTAQ
16	ReadTAC register to read time output	16	Read_TAC	out _OTAQ
32	trigger delayed + not delayed outputs (channel 0 to 15) : T_delay ch0 +T ch0 + T_delay ch1 + T ch1 + …+T_delay ch15 +T ch15	32	probe_dig	T_delay-->dig2 + T -->dig1
32	2 digital signals for TAC (channel 0 to 15) : sel_colb2 (ch0) + sel_colb1 (ch0) + ... +sel_colb2(ch15)+sel_colb1(ch15)	64	probe _tac	sel_colb2-- >dig2+sel_colb1-->dig1
80	5 digital signals for SCA (channel 0 to 15) (note 1) : T&HQ2 + T&HQ1 + T&HT2 + T&HT1 + col2toRead (ch0) + …… + T&HQ2 + T&HQ1 + T&HT2 + T&HT1 + col2toRead (ch15)	96	probe _sca	dig2+dig1 (note1)
48	Slow shapers + fast shaper outputs (channel 0 to 15) : Ssh_lg_ch0 + fsh_ch0+ssh_hg_ch0+ …+ ssh_lg_ch15 + fsh_ch15+ssh_hg_ch15	176	probe_sh	analog
32	Preamp low gain and high gain outputs (channel 0 to 15) : pa_lg_ch0 + pa_hg_ch0 + pa_lg_ch1+pa_hg_ch1 +… + pa_lg_ch15 +pa_hg_ch15	224	probe_pa	analog
2	TDC start_ramp1 + start_ramp2	256		ramp1-->dig1 + ramp2 -->dig2
2	TDC out_ramp2 + out_ramp1	258		analog
260				
note 1 probe SCA : signals : T&HQ2 + T&HQ1 + T&HT2 + T&HT1 + col2toRead output probe : dig2 + dig1 + dig2 + dig1 + dig1				

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